

**Massachusetts Institute of Technology**  
**Center for Space Research**  
**Cambridge, MA 02139**  
**Room 37-558**

To: ACIS Team  
 From: Beverly LaMarr (fergason@space.mit.edu)  
 Subject: Measured CTI vs Detected ACIS Counts During External Calibration Source Data Sets  
 Date: 06 January 2000

The measured CTI of the ACIS front illuminated devices has been increasing from day 264 to day 353. The upper left panel of Figure 1 shows the average measured CTI of the four I chips apparently increase by nearly 4% over three months.

At the same time, the number of events rejected because they have a pulse height greater than 3750 ADUs (approximately 15keV) has been decreasing. The upper right panel of Figure 1 shows the average detected events above 3750 ADUs of the four I chips decrease by about 13%.

The lower left panel of Figure 1 shows the average measured CTI of the four I chips plotted against the average detected events above 3750 ADUs per frame for S3. The high energy events for the S3 device was used because there is no apparent change in its measured CTI (see the upper left panel of Figure 1).

Table 1 summarizes the slope and intercept of a linear fit to the CTI vs S3 high energy count rate for each device

Chip	Intercept	Slope
i0	17.51	-0.0516
i1	17.41	-0.0469
i2	20.62	-0.0536
i3	20.85	-0.0550
s0	28.30	-0.0548
s2	23.49	-0.0428
s4	19.77	-0.0439
s5	21.32	-0.0467
s1	1.83	0.0012
s3	1.17	-0.0019

Table 1: Fit of CTI vs S3 High Energy Count Rate

Using the linear fits presented in Table 1, each measured CTI value was corrected to the same flux rate. The lower right panel of Figure 1 shows the average of the four I chips CTI corrected to an S3 high energy count rate of 60 counts per exposure.

Because a higher flux rate (filling more pixels with sacrificial charge) is known to reduce the measured CTI, it is reasonable to assume that the apparent decrease in background is real and is the cause of (at least part of) the apparent increase in the CTI. This could be proven with an experiment using the flight instrument where external calibration source data are collected with varying exposure times. It is important to understand this relationship to correctly use CTI measurements to monitor damage to the devices.

Plots similar to those described above for each of the ten flight devices are included as Figures 2 through 11, with plots for the two back-illuminated devices (s1 and s3) last.

At this time the poorer correlation for the front illuminated S-array chips is not understood.

The high energy count rate for each device is taken from the exposure records telemetered by the instrument. All data presented here were taken with the focal plane temperature set at -110C.

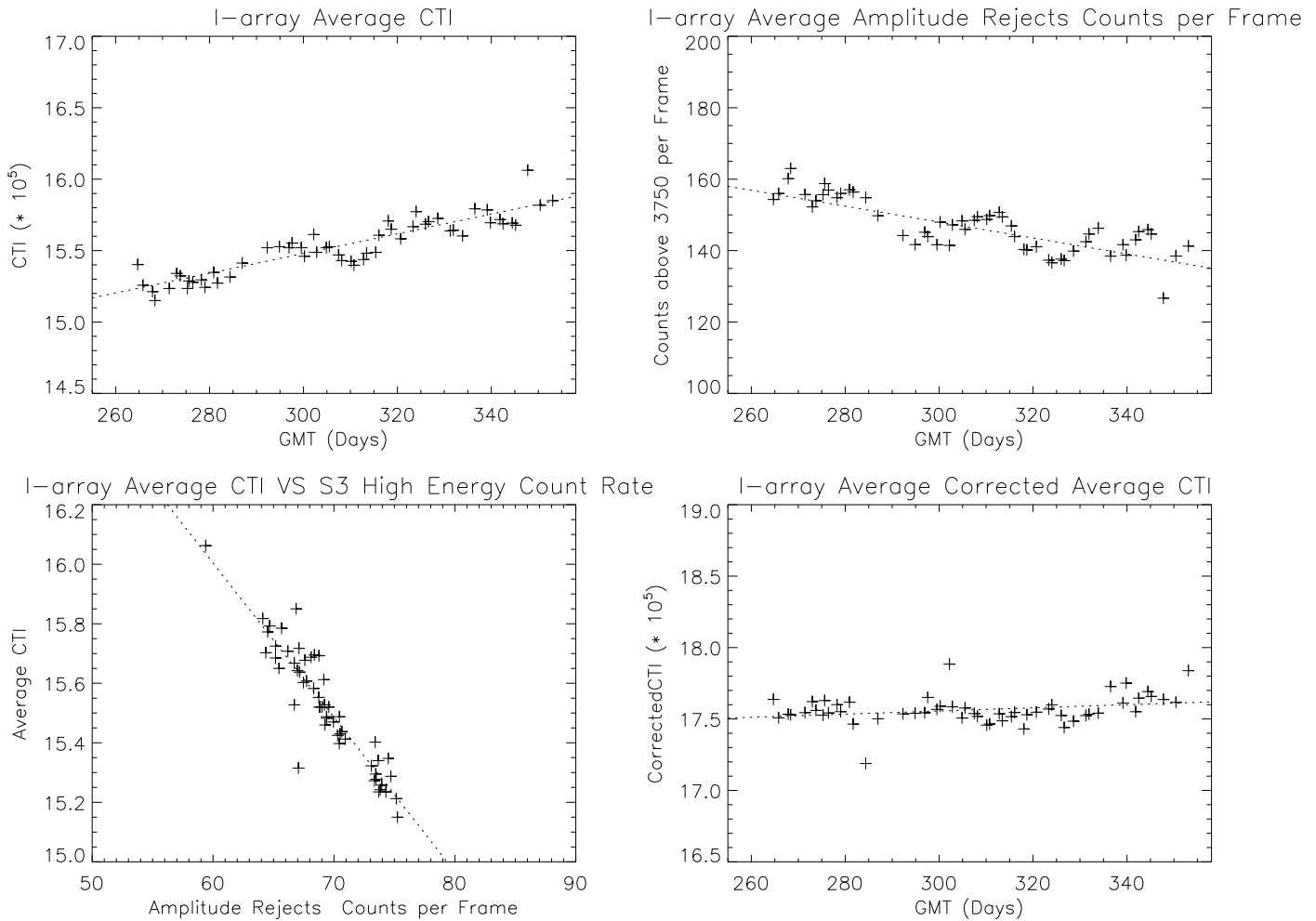


Figure 1: I-array Average CTI vs Count Rate

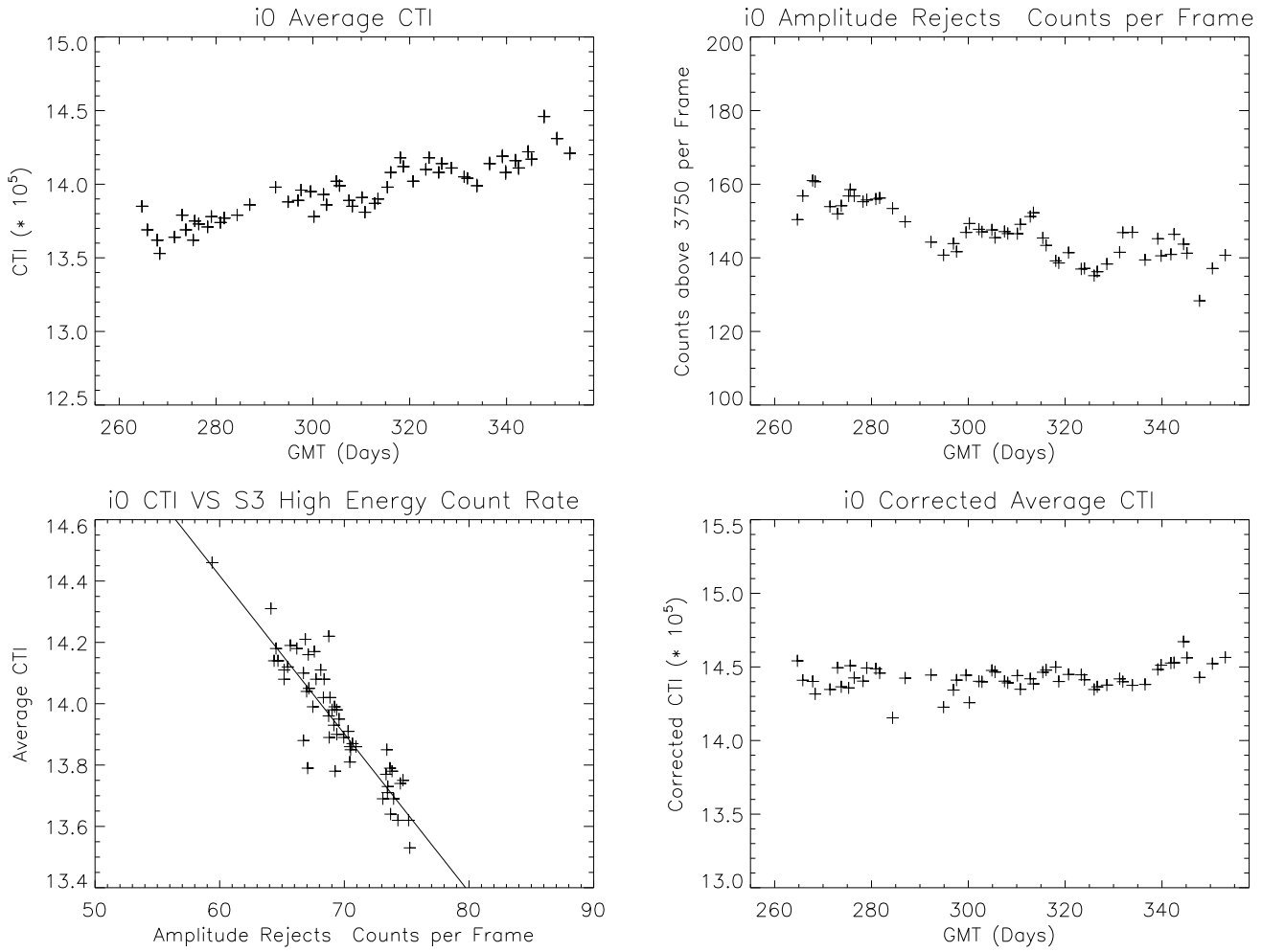


Figure 2: I0 CTI vs Count Rate

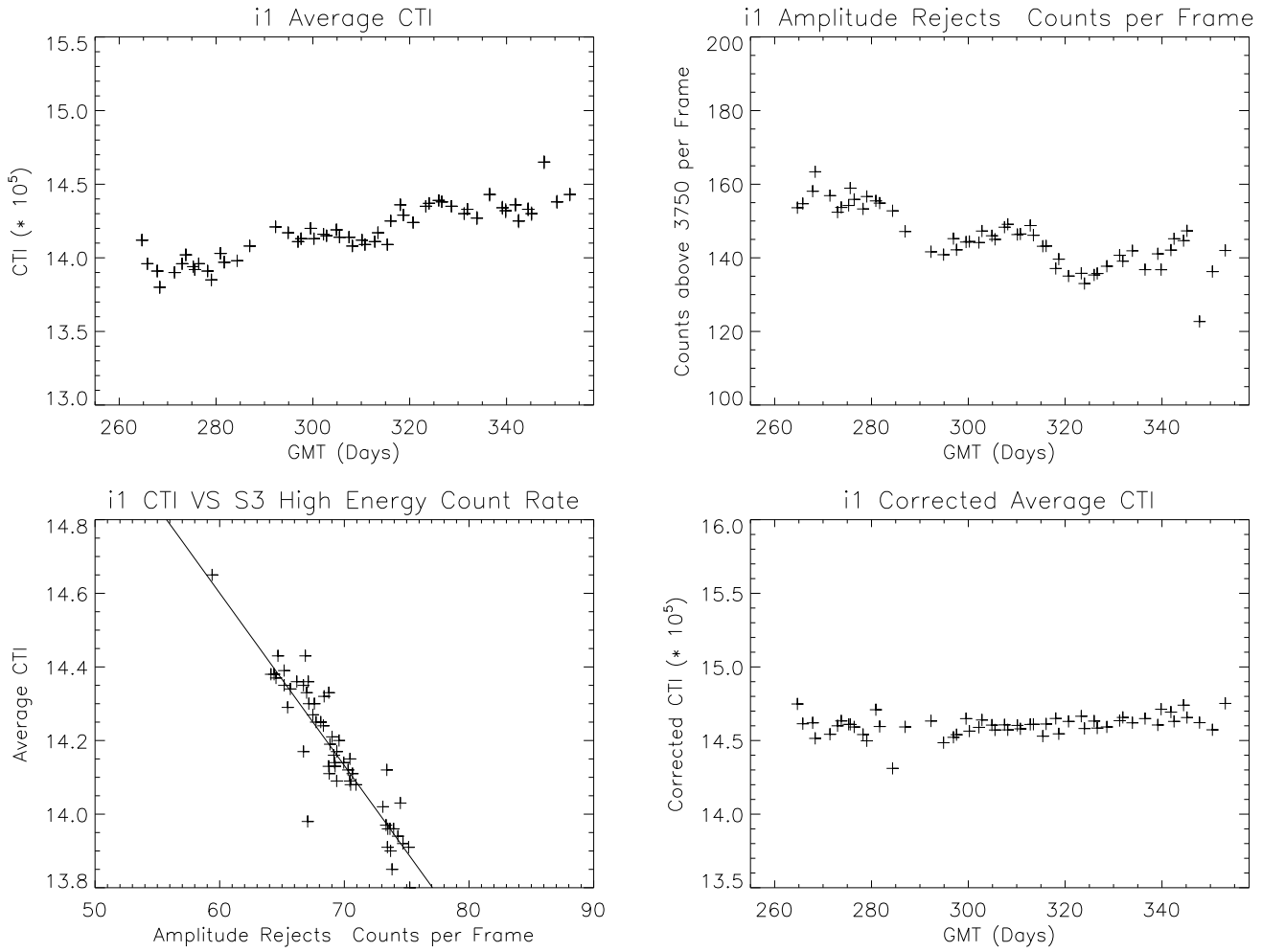


Figure 3: I1 CTI vs Count Rate

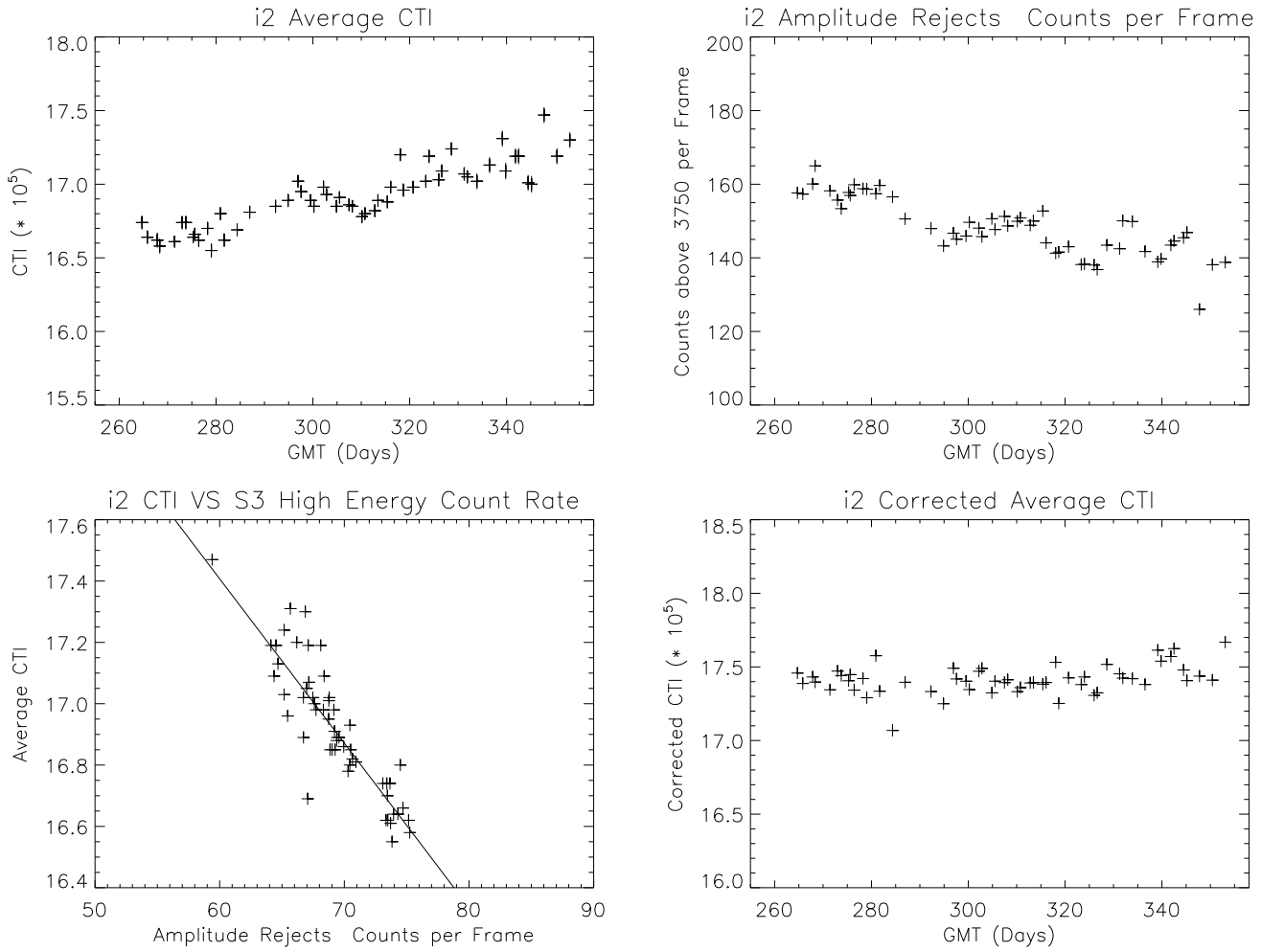


Figure 4: I2 CTI vs Count Rate

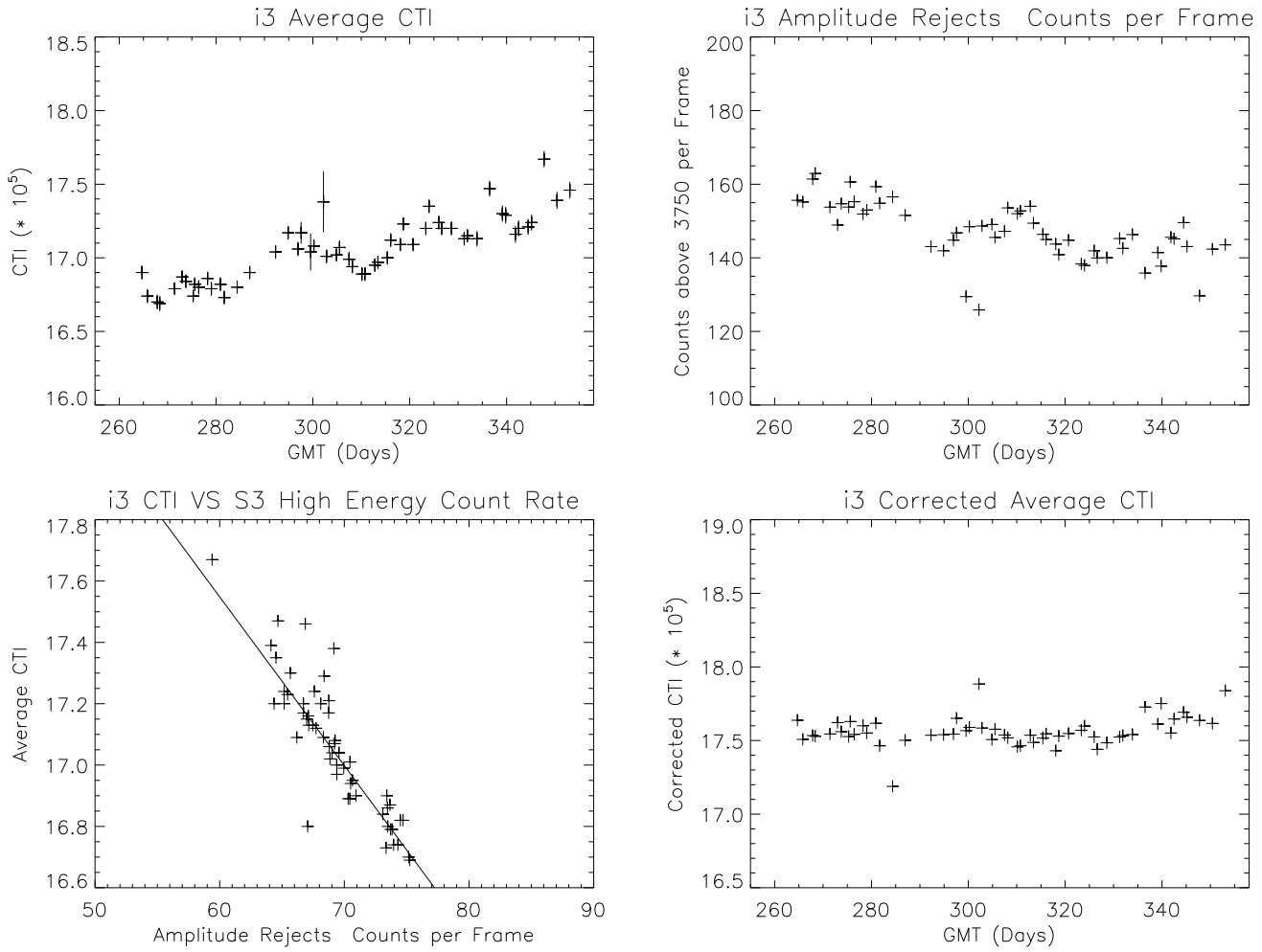


Figure 5: I3 CTI vs Count Rate

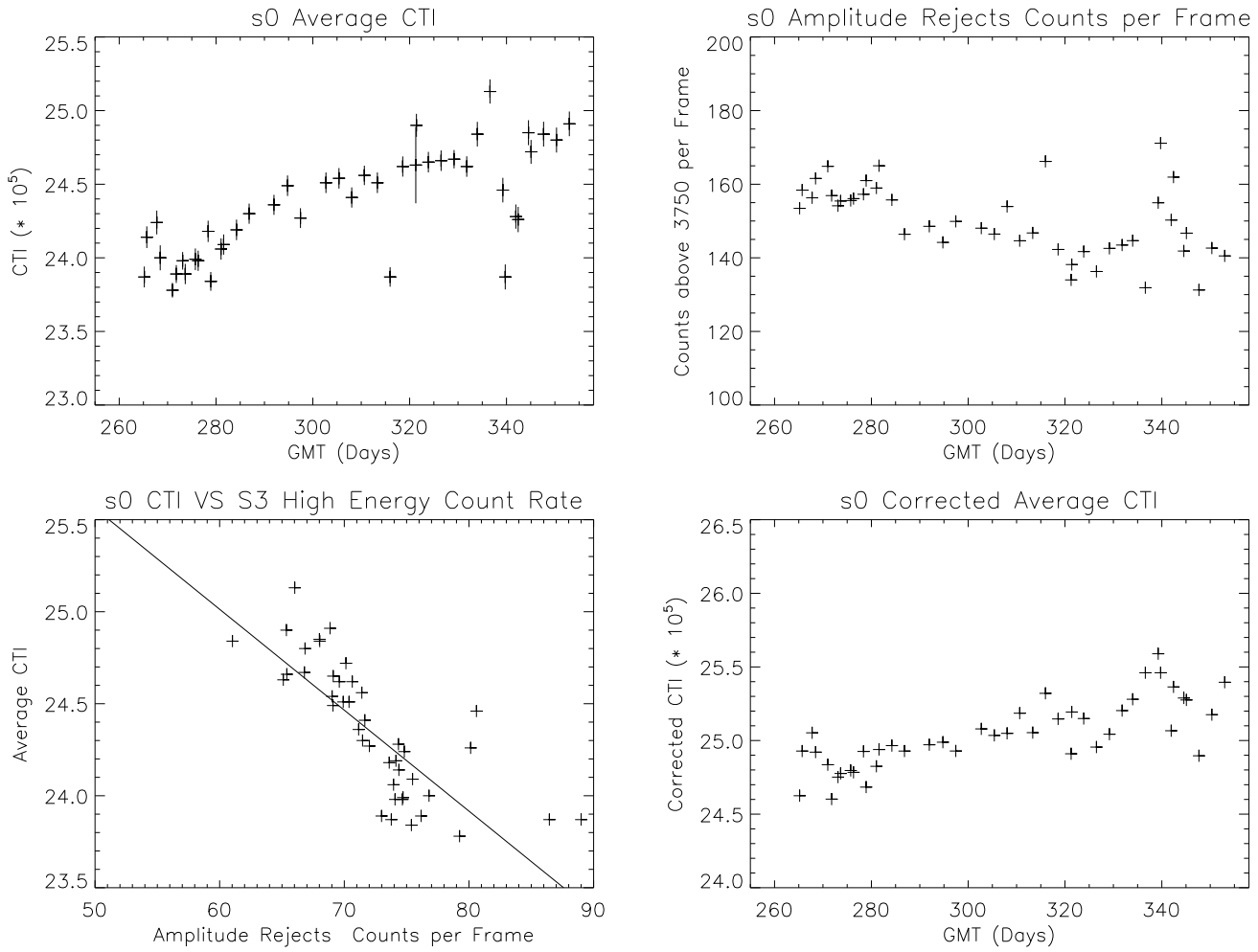


Figure 6: S0 CTI vs Count Rate

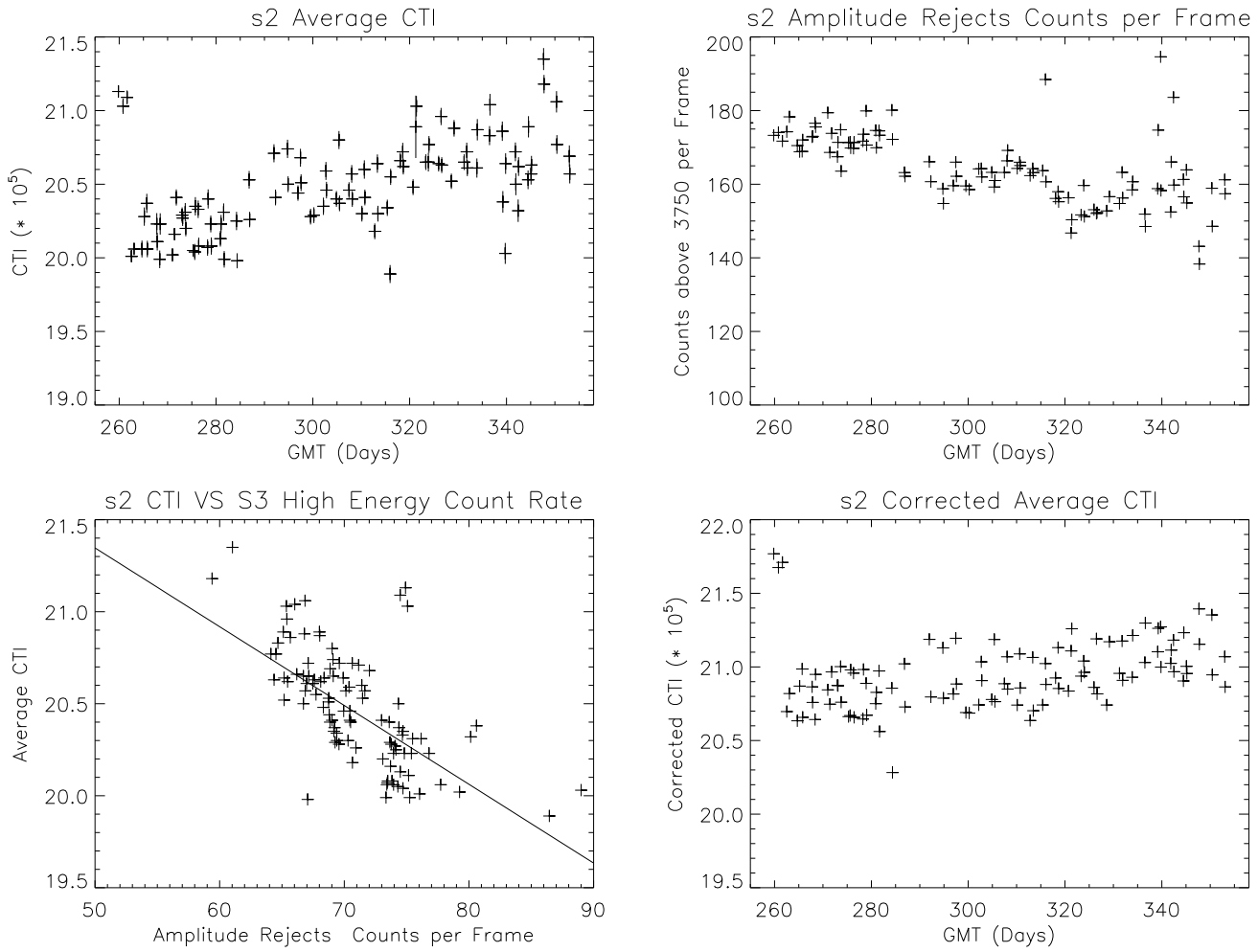


Figure 7: S2 CTI vs Count Rate



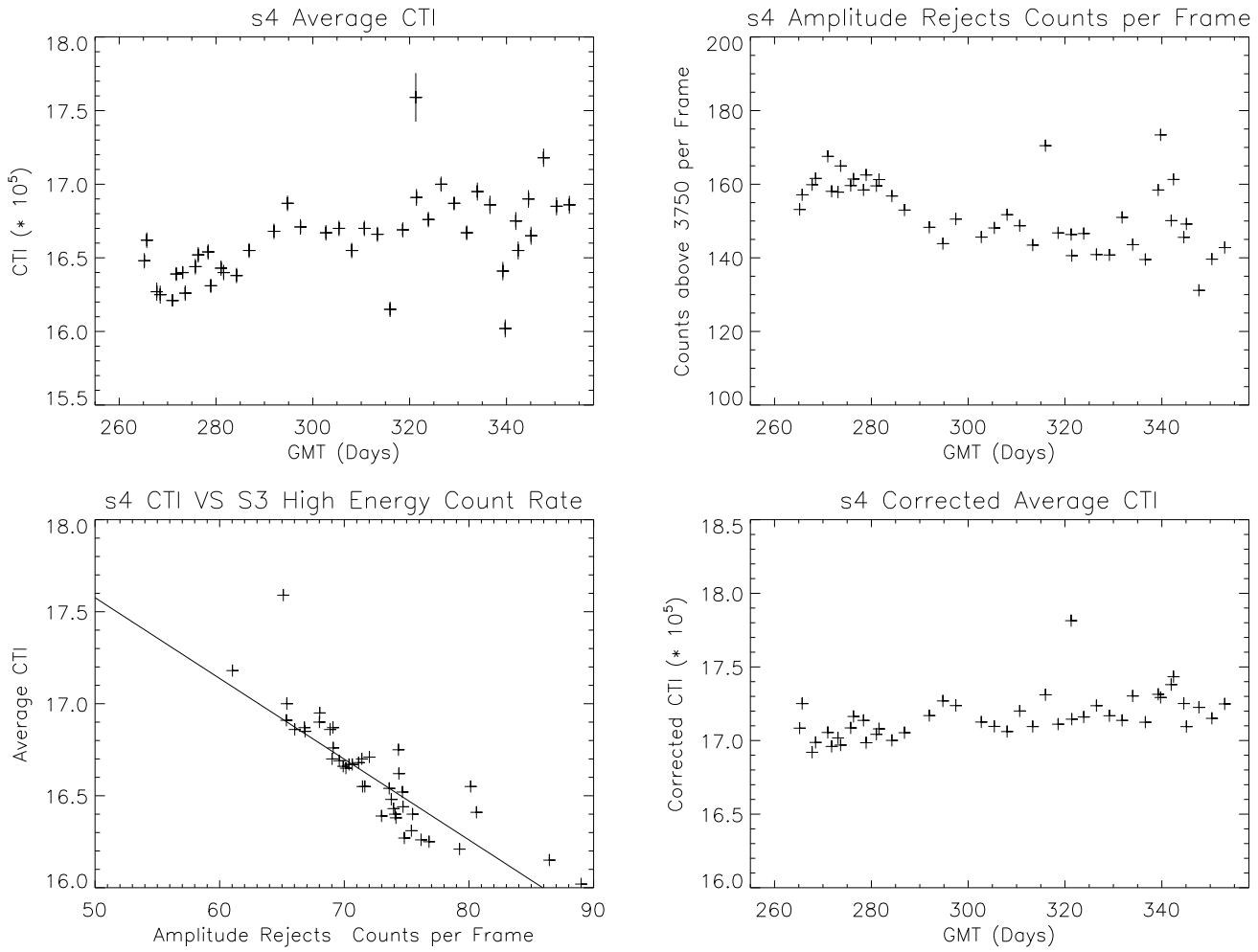


Figure 8: S4 CTI vs Count Rate

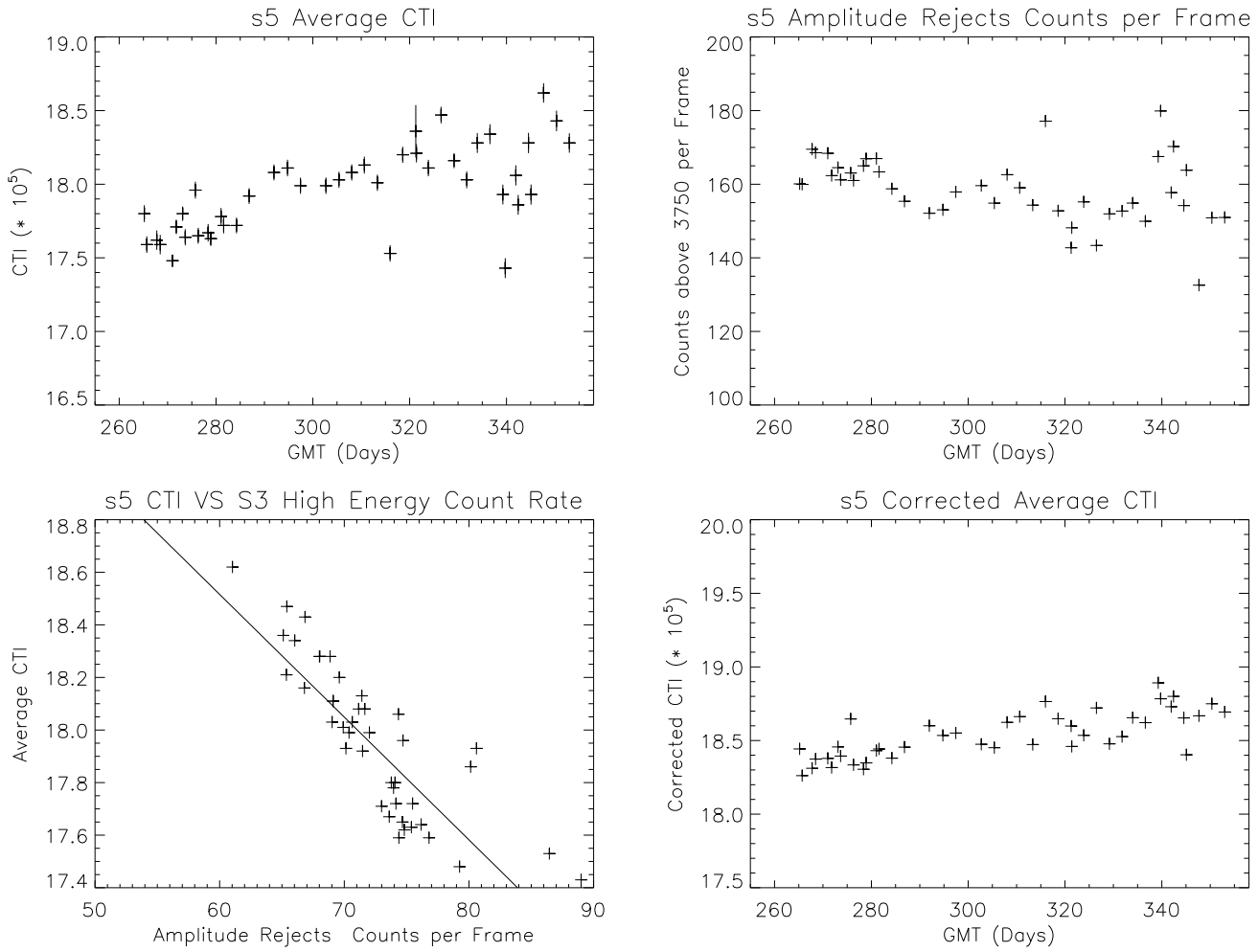


Figure 9: S5 CTI vs Count Rate

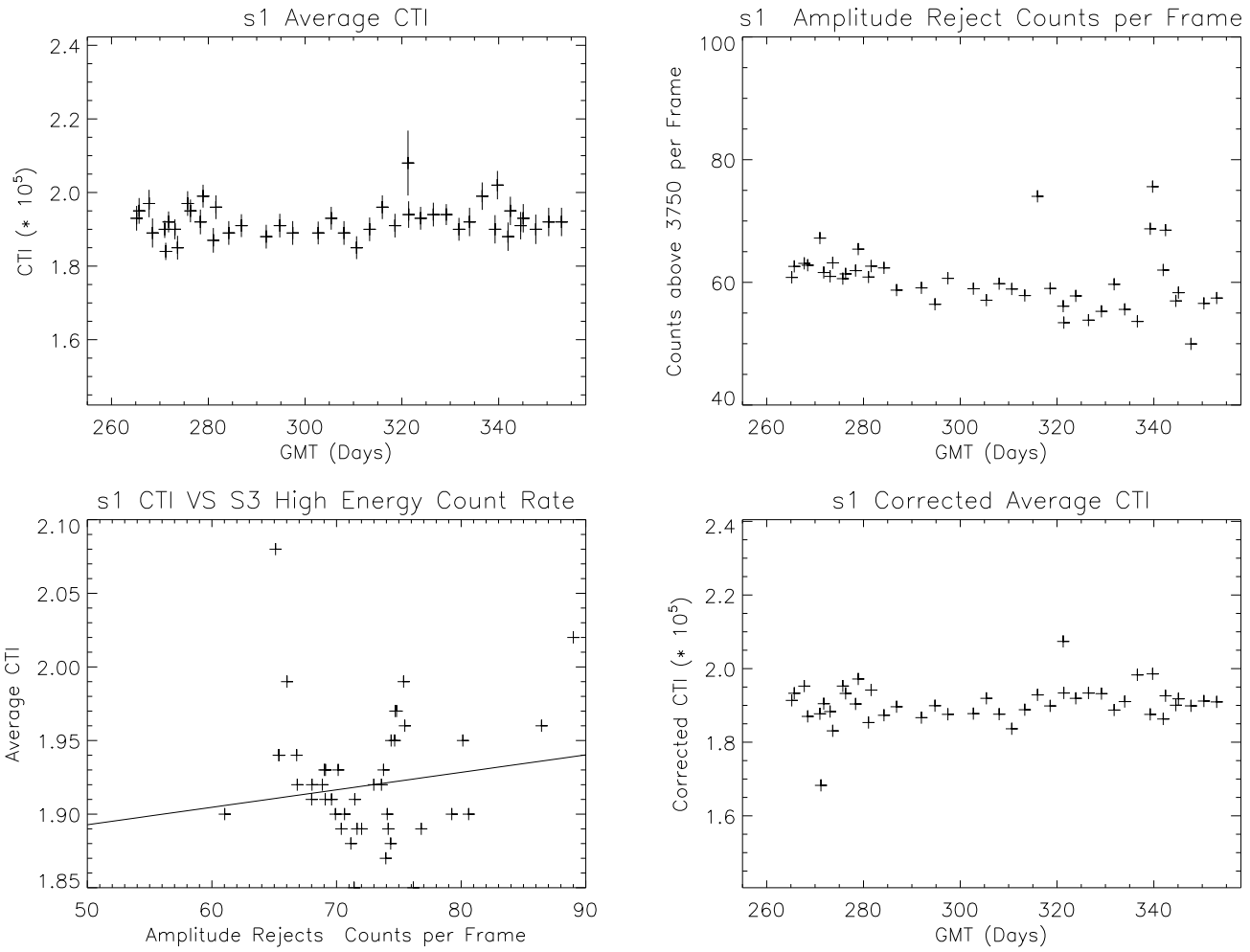


Figure 10: S1 CTI vs Count Rate

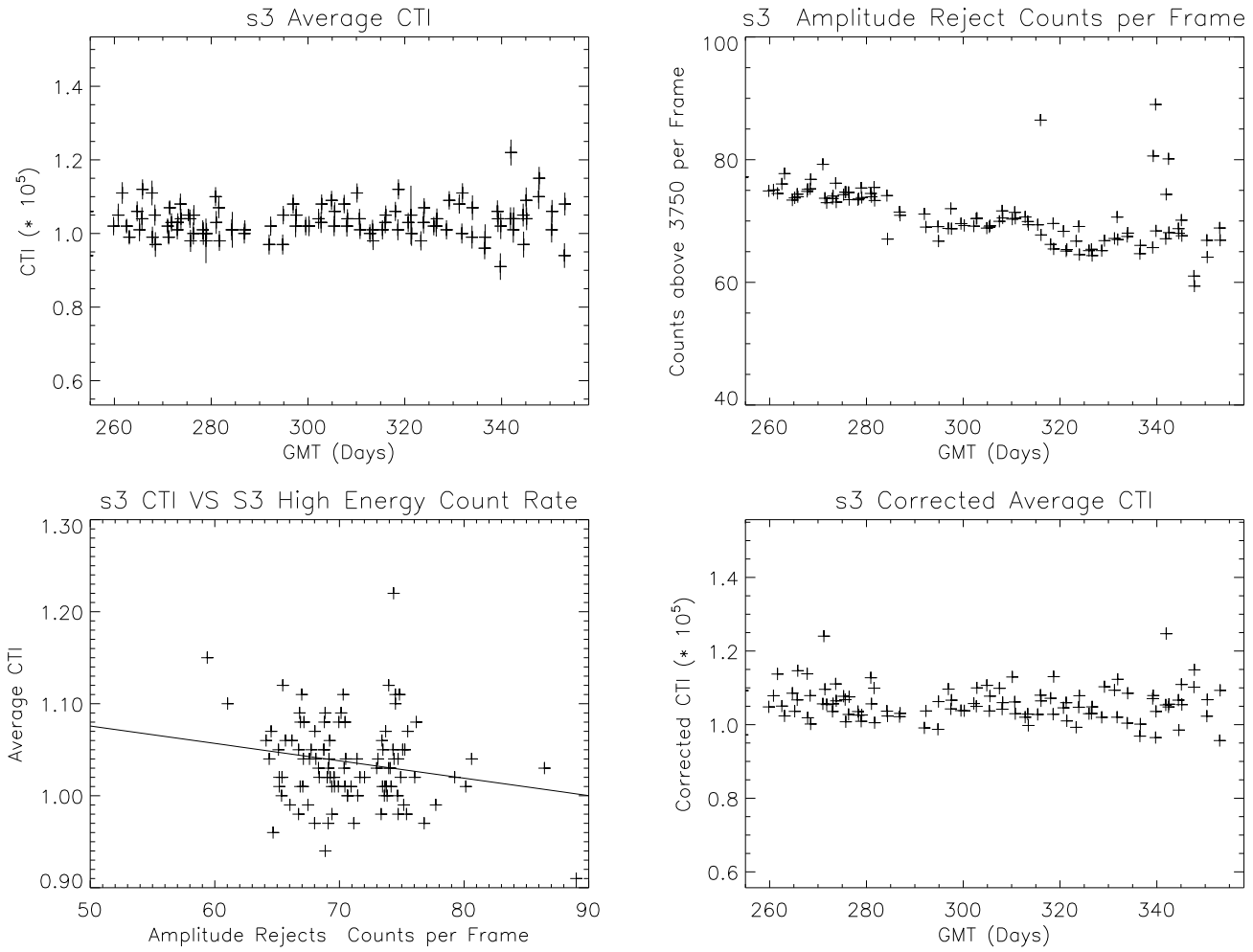


Figure 11: S3 CTI vs Count Rate