Abstract—We describe the key features and performance data of a 1024 × 1026-pixel frame-transfer imager for use as a soft-X-ray detector on the NASA X-ray observatory Advanced X-ray Astrophysics Facility (AXAF). The four-port device features a floating-diffusion output circuit with a responsivity of 20 μV/e⁻ and noise of about 2 e⁻ at a 100-kHz data rate. Techniques for achieving the low sense-node capacitance of 5 fF are described. The CCD is fabricated on high-resistivity p-type silicon for deep depletion and includes narrow potential troughs for transfer inefficiencies of around 10⁻⁵. To achieve good sensitivity at energies below 1 keV, we have developed a back-illumination process that features low recombination losses at the back surface and has produced quantum efficiencies of about 0.7 at 277 eV (carbon Kα).

I. INTRODUCTION

Currently, CCD imagers are well-established as soft-X-ray spectroscopic detectors. This technology, with the combination of low noise (2 e⁻), large area, and mechanical ruggedness, has eclipsed the tube-based technologies such as the gas-scintillation proportional counters. The best solid-state detectors, such as Si(Li) detectors, have higher noise and must operate at lower temperatures than CCD's. Two CCD focal planes based on four-chip 420 × 420-pixel imager mosaics have now been operating for four years in the US/Japanese Advanced Satellite for Cosmology and Astrophysics (ASCA) [1]. Here, we describe the further development of CCD's for use in the Advanced X-ray Astrophysics Facility (AXAF) satellite [2]–[4].

For the AXAF sensors, several aspects of the earlier ASCA devices were improved. Primary among these were lower read noise, larger area devices, and better response at lower (<1 keV) energies. The packaging technology for AXAF has been in itself a major development but will not be described here. Improved read noise has resulted from an output circuit design which, among other things, utilizes buried contacts for a more compact sense node with reduced capacitance. The devices described here have a die size approximately four times larger than those of ASCA, and this was made possible by a transition from 75- to 100-mm wafers and a move from a class-100 fabrication facility to a new facility with near class-1 conditions. For improved low-energy response, we used a back-illumination process to avoid the large X-ray absorption losses below 1000 eV in the gate and dielectric layers of front-illuminated devices.

II. DEVICE DESIGN

A. Architecture and Process Overview

The architecture of the device, which is illustrated in Fig. 1, builds on the predecessor 420 × 420-pixel ASCA device and is likewise three-side abutable. The sensor is made with a three-phase, triple-polysilicon process that has been described earlier [2], and the pixel sizes are 24×24 and 13.5 (V) × 21(H) μm in the imaging and nontapered frame-store regions, respectively. The frame stores are partitioned into left and right sections,
The low bulk dark current is indicative of the good silicon wafer quality available at these high resistivities. For this application, the devices are to be operated at temperatures below $-100\,^\circ C$ and frame times of less than 10 s, and under these circumstances, the dark current per pixel is well below $1\, e^-/\text{pixel/frame}$.

Fig. 3 is a photograph of an assembled 10-chip focal plane for AXAF and is the core of the CCD camera system called ACIS (AXAF CCD imaging spectrometer). It comprises a $2 \times 2$ imaging array and a $1 \times 6$ spectrometer array of chips for detection of X-rays from an energy-dispersive grating. The frame stores are covered by X-ray opaque plates. The $2 \times 2$ imaging-array devices are tilted to best match the highly curved focal surface of the AXAF mirror assembly. Two devices of the spectrometer array will be back illuminated in the flight focal plane.

B. Radiation Hardening

An essential feature of any CCD to be operated at low signal levels in space is radiation hardening. The principal source of radiation damage are high-energy protons that produce displacement damage. This damage manifests itself as trapping centers, principally the P-V center [6], [7], which increase the charge-transfer inefficiency (CTI). For this application where the signal levels are very low, the performance is extremely sensitive to such traps. The standard method of hardening a CCD is the so-called trough [8]–[10]. The trough is a region of higher potential in the form of a narrow stripe down the center of the channel and is created by an additional donor implant (for n-channel devices). Typically, the potential in the trough is 1.5–2 V higher than in the surrounding buried channel. Small charge packets will be confined to this narrower channel and will therefore encounter fewer traps during transfer. The ASCA devices used $2\mu m$ wide troughs in the imaging and frame-store sections, and the same trough width has been used in the device described here. The charge capacity of the trough is well above 10,000 $e^-$, and therefore, even the maximum X-ray event charge of around 3000 $e^-$ is readily contained within the trough. As expected, the narrower the channel, the more radiation tolerant the device will be [11], but this is limited by the capabilities of the available lithography and by the lateral diffusion of the dopant during subsequent high-temperature steps. Since the $2\mu m$ trough has more than sufficient charge capacity, it is clear that a narrower trough would be more desirable for this application.

Another hardening technique is to operate the device at temperatures of about $-120$ to $-130\,^\circ C$, where there is a minimum in the CTI of an irradiated device, and the AXAF CCD’s are to be operated around this temperature. This CTI minimum arises because at this temperature, the emission times of the P-V centers are very long compared to frame times, while other radiation-induced traps apparently have very fast emission times compared with charge-transfer rates and are therefore not effective in increasing the CTI.

One interesting design issue with the trough concerns the interface between the frame store and serial register, where the charge must make a $90^\circ$ turn. For process simplicity, it

![Fig. 2. Layout of the midpoint of the serial register illustrating (a) bidirectional and (b) unidirectional clocking possibilities.](image)

and each frame store feeds a serial register with output ports on both ends. The serial register is split in half with mirror symmetry about the center line. This symmetry also extends to the output circuit, and this minimizes the number of design cells as well as helping to maintain close matching of the performance under identical bias and clocking conditions. Fig. 2 illustrates the layout at the center line. Five serial clock lines are brought out to pads. Depending on how these lines are clocked, the charge can be transferred entirely to the left or right port or half to each port. This operational flexibility was considered to be important for the sake of redundancy should one or the other amplifier or its video chain fail.

The devices are fabricated on high-purity p-type float-zone wafers with resistivities of about 7000 $\Omega \cdot cm$. Such high purity is needed in order to achieve the deep depletion depths essential for good spectroscopic performance at the higher X-ray energies (6–10 keV), where the photon penetration depths become very long. Depending on clock levels, the depletion depths range from about 50 to 70 $\mu m$. Unfortunately, float-zone silicon is vulnerable to the generation of plastic slip and dislocations and requires special processing techniques that limit thermally induced stresses during high-temperature processes [5]. Czochralski silicon, by virtue of its higher oxygen content, is not nearly so vulnerable, but such silicon is not available at the low dopant levels required of this application.

Room temperature dark currents are typically about 500 pA/cm$^2$, of which the contribution from the bulk is about 50 pA/cm$^2$, and the remainder is surface-state dark current.
is desirable to place the entire trough in a single mask level. In one such design, the parallel trough was terminated at the bottom edge of the frame store, and a separate trough was placed horizontally in the serial register [10]. Our concern here was the potential barrier at the terminated end of the parallel trough, which, unless precisely aligned with a gate edge, could have led to trapped charge behind the barrier. In the ASCA devices, the serial register was unidirectional, and we were able to merge the parallel and serial troughs in a fairly straightforward way with a continuous trough that more or less followed the charge flow path from the parallel to serial registers [12]. In the present device, the serial register is bidirectional, and a single-level trough design was more difficult. A simple T-shaped trough was considered, but during clocking of the serial register, it was thought that charge in the arm of the T reaching up to the frame store would be subject to relatively weak drift fields and would empty rather slowly into the main horizontal serial trough.

The design that we used, which is illustrated in Fig. 4, is a kind of modified T in which the junction of the arms was moved up closer to the frame store. One of the pitfalls in designing such structures is the narrow-channel effect, which can create potential wells or barriers and seriously degrade transfer efficiency at points where the trough becomes wider.
or narrower. At the trough junction, the trough becomes wider than the arms, and this could result in a deeper potential well or pocket that could trap charge. To avoid this, the junction was placed at the boundary between the phase-1 and phase-2 gates so that the high lateral E-fields would override the narrow-channel effect. The arms of the trough in the serial register were made 3-μm wide to also minimize this effect. The wider serial trough could be tolerated even though it does not give as much radiation hardening as the 2-μm parallel trough because there are fewer serial charge transfers. The design in Fig. 4 works well for serial clock rates up to at least the highest tested clock rate of 1 MHz.

C. Output-Circuit Design

When the dark current is negligible and the CTI is perfect, the energy resolution $\Delta E$ expressed as full width at half-maximum (FWHM) of the device for photons of energy $E$ is determined by the Fano noise, which is the fundamental statistical fluctuation in the photoelectron count, and the device read noise according to the formula

$$\Delta E = 2.355E_p\left(F+E_p + N_F^2\right)^{1/2}$$  \hspace{1cm} (1)

where

- $F \cong 0.12$ Fano factor for silicon;
- $E_p \cong 3.69$ eV average energy needed to create one electron-hole pair at $T = -120^\circ$ C [13];
- $N_F$ read noise in electrons.

The Fano noise at the important carbon K line (277 eV) is equivalent to about 3 e$^-$, and therefore, the read noise should be below this level in order to maintain Fano-noise-limited performance over the whole energy range of AXAF.

To improve on the read noise of the ASCA devices, design and process changes were made in the output circuit to reduce parasitic capacitances at the charge sense node. The design change with the biggest process impact was a change in the
manner by which the sense MOSFET gate was connected to the floating n\textsuperscript{+} diffusion. Fig. 5(a) shows a photo of the earlier method of making this connection. First, an n\textsuperscript{+} diffusion was formed, followed by the gate polysilicon which, after etching, partially overlapped the n\textsuperscript{+}. Next, both a contact window and a metal strip that straddle the polysilicon gate and the n\textsuperscript{+} region are formed. The compounded effects of the several alignment tolerances and design rules resulted in a structure that was not optimum for minimizing parasitic capacitances. A more compact and lower-capacitance method is illustrated in Fig. 5(b), where the polysilicon gate is connected to the substrate via a buried contact [14]. To form this connection, a contact window is etched in the oxide/nitride gate insulator prior to the polysilicon deposition. The polysilicon is then deposited and doped, and in this way, a self-aligned n\textsuperscript{+} floating diffusion is formed. This approach is simpler for the output circuit and involves the careful alignment of fewer levels than the butt contact of Fig. 5(a), although it requires an additional mask level to the overall process.

One drawback of the buried contact is the need to minimize the native oxide between the polysilicon and the substrate to ensure good electrical contact. For this purpose, the wafers are briefly etched in a dilute HF solution just prior to the furnace loading for the polysilicon deposition. However, the HF can attack weak spots in the oxides of the previous polysilicon layers and the gate insulator and lead to shorts involving the polysilicon to be deposited. This has not been a problem except when the polysilicon oxides of the preceding layers are not sufficiently thick.

Another method of reducing the parasitic capacitances of the floating diffusion circuit has also been described [14] and is illustrated in Fig. 6. Here, the buried-channel implant is masked from regions between the MOSFET gate and floating n\textsuperscript{+} formed by the buried contact and the channel stops, except for a 2-\textmu m “funnel” that guides charge onto the n\textsuperscript{+} from the output gate and out through the reset transistor. In the conventional approach, this implant is not masked, and the n-buried-channel implant fills all gate-insulator regions and
abuts the channel-stop $p^+$ region. In the present case, the portion of the polysilicon gate around the buried contact is isolated from the channel stop by as much as 3 $\mu$m of lightly-doped $p$ substrate. An additional measure for reducing parasitic capacitances is the 2.5-$\mu$m separation between this portion of the polysilicon and both the output and reset gates, using only a 2-$\mu$m wide lightly doped (by the n-buried-channel and trough implants) region to carry charge to the sense node and off through the reset transistor. Generally, we have not experienced any adverse spurious surface dielectric charge effects over these lightly doped regions and have not used field plates over this node to control surface charge. However, when the exposed channel between output gate or reset gate and the polysilicon at the buried contact is 3 $\mu$m or more, the channel will sometimes pinch off due to surface charging effects. Spacings of 2.0 and 2.5 $\mu$m are also used between the FET gate and the source and drain $n^+$ regions of the FET to minimize gate capacitances [2].

The combination of buried contact and the charge funnel have reduced the capacitance from about 10 to 5 fF, and the corresponding responsivities have increased from 10 to 20 $\mu$V/e$^-$. The typical noise performance for the ASCA devices was 4–5 e$^-$ operating at a 50-kHz data rate, whereas the higher-responsivity devices here typically measure 1.8–3 e$^-$ at 100 kHz, as shown in Section IV.

III. BACK ILLUMINATION

As X-ray energies drop below about 1 keV, the absorption lengths in silicon, oxygen, and nitrogen become very short, and the polysilicon and insulator layers on the device surface absorb significant amounts of the radiation. Fig. 7 shows the X-ray absorption lengths for two of the three dead-layer components on the front of the device. The device layer thicknesses average 0.33 $\mu$m for the polysilicon gates, 0.29 $\mu$m for the SiO$_2$, and 0.04 $\mu$m for the Si$_3$N$_4$. Thus, the X-ray absorption length is roughly equal to the dead-layer thicknesses at about 700 eV so that at this energy the quantum efficiency would be about 0.37. Below this energy, the front-illuminated quantum efficiency will decline significantly to only a few percent at the carbon line. Back illumination is one solution to this problem, provided a) the recombination losses at the back surface can be minimized, and b) strong drift fields can be established through the device all the way to the back surface. The latter is important for minimizing lateral diffusion of the event charge, which otherwise can lead to charge splitting among several pixels when the charge arrives at the front surface. Such split events degrade the energy resolution because the event charge must be computed by summing signals from two or more pixels, each of which has been degraded by the read noise. The ideal structure is illustrated by way of a band diagram in Fig. 8. The device is fabricated on lightly doped material for fully depleted conditions. At the back surface, a shallow $p^+$ layer is introduced to provide a field that repels electrons away from the back surface.

The fabrication process for such a device is outlined in Fig. 9. The wafer is mounted in a fixture that protects the front surface and a narrow rim (approximately 3–5 mm wide) around the perimeter of the back surface. The back surface is etched in a mixture of nitric, acetic, and hydrofluoric acids until the desired thickness, typically 40–45 $\mu$m, is achieved without the need for etch selectivity. This thickness is measured using Fourier-transform infrared transmission and is typically uniform to within $\pm 2\mu$m. The back surface is implanted with BF$_2$, and the wafer is annealed. In addition, a layer of SiO$_2$ is grown on the back. Fig. 10 shows the measured concentration profile of boron after all processing is completed. The wafer is finally bonded face down on a support wafer using epoxy, and after masking, the silicon and oxide layers on top of the bonding pads are etched away using dry etching techniques.

A measure of the recombination losses on the back surface is the internal quantum efficiency in the ultraviolet. Fig. 11 shows the measured quantum efficiency versus wavelength from 225 to 400 nm for a device with a 35-nm thermal oxide layer, as well as a calculated curve for which the internal quantum efficiency was assumed to be 100%. Over
this wavelength band, the absorption lengths drop as low as 4 nm, which is well within the field-free portion of the p+ layer. The agreement between measured and calculated curves indicates very low recombination losses either from the surface states or the p+ layer.

IV. PERFORMANCE AS AN X-RAY SENSOR

After fabrication, but before installation in the ACIS instrument, each device is subjected to detailed characterization and X-ray calibration measurements [3], [15]. In this section, measurements of CTI, noise, spectral resolution, and X-ray quantum-detection efficiency of typical devices are presented.

The demanding CTI requirement is driven not only by the sheer size of the device (as many as 2312 pixel transfers) and the extreme sensitivity of the energy resolution to CTI but also by the need for a margin of deterioration due to on-orbit radiation damage. CTI in the low-10^-6 range, measured under low-level X-ray illumination, was desired at the outset of the program. Fig. 12 shows the results of parallel CTI measurements for a typical front-illuminated flight candidate device at a temperature of -120 °C. Following Janesick et al. [16], the measured amplitudes of Mn Kα X-rays are plotted as a function of event location in the device. A fit to the data for each quadrant shows that there is essentially no measurable change in amplitude with position; the CTI measurement uncertainty is about 3×10^-7 (1σ). For clarity of presentation, only events with amplitudes within three standard deviations of the most probable event amplitude are plotted.

Noise histograms, which are computed from pixel-by-pixel differences of two successive frames read from one device, are shown in Fig. 13 for each output node. ACIS prototype electronics are used for these measurements, and although the electronics typically contributes about 1–1.5 e^- noise (at the preamp input), it is possible that additional nondevice noise is coupled into the video from the cabling leading into the test chambers and that the true device noise is lower than the values reported here. The figure shows a Gaussian distribution fit to data from both the imaging pixels and, for comparison, the overscan pixels from the serial readout. The readout noise, which is computed by dividing the best-fit standard deviation by √2, is also shown. RMS noise of order 2 e^- is typical of ACIS flight candidate devices. The noise distributions are accurately Gaussian over four orders of magnitude, and the influence of a bright column defect in one quadrant can be seen as a tail in the histogram of quadrant D.

The excellent noise and CTI performance result in very good X-ray spectral resolution. Fig. 14 shows the measured spectral resolution ΔE from 525 to 9900 eV. Using (1), the best-fit value of the readout noise is 2.2 electrons, which is...
consistent with noise histogram measurements. The spectral resolution at 525 eV is better than 50 eV. The fitting parameter $FE_p = 0.490$ used in the figure agrees reasonably well with the value of 0.443 based on the estimated value of $F = 0.12$ and $E_p = 3.69$ eV.

The back-illuminated devices exhibit charge-transfer efficiency, noise, and spectral resolution that are somewhat poorer than that of the front-illuminated devices. The CTI of the best back-illuminated devices is at least $1 \times 10^{-5}$ per transfer. Readout noise is typically 4–5 e$^-$ rms, principally because the gain of the output amplifiers is somewhat lower on the back-illuminated devices. This is possibly the result of capacitive loading on the output circuit due to the proximity of the substrate wafer to which the thinned device wafer is epoxied. Spectral resolution of the back-illuminated devices at energies below 1500 eV is 100–120 eV, FWHM, and nearly independent of energy. This higher $\Delta E$ cannot be explained by the higher noise and CTI and is surprising in light of the known low recombination losses at the rear surface where photons at these energies are absorbed.

The measured detection efficiencies of front- and back-illuminated devices are compared in Fig. 15, and the superior low-energy detection efficiency of the back-illuminated device is obvious. The front-illuminated device, as suggested earlier by the discussion of Fig. 7, shows a declining quantum effi-

ciency with energy. The back-illuminated device also shows some decline associated with the 35-nm thermal SiO$_2$ layer on the back surface. The rapid variation of the quantum efficiency near the oxygen K$_\alpha$ absorption edge at 525 eV is due to X-ray absorption fine structure in the oxide dead layers of the devices [17]. One can also see a small variation in the front-illuminated data at 392 eV from the nitrogen K$_\alpha$ absorption in the gate nitride.
Fig. 13. Noise histograms from each of the four quadrants of a device at -120 °C. For comparison, the noise is measured both in the imaging pixels and in the overclocked pixels during serial readout.

Fig. 14. Measured energy resolution as FWHM on a front-illuminated device over the ACIS energy range. The solid line is a best fit of (1).

V. SUMMARY

The design, fabrication, and performance of a 1×1 k imager to be used as a soft-X-ray sensor on the AXAF satellite have been described. The design of the output circuit has resulted in noise levels around 2 e^- at a 100-kHz data rate, resulting in excellent energy resolution over the energy band from 300 to 10,000 eV. Careful processing of the high-purity float-zone silicon and the use of a narrow trough in the center of the CCD channel has resulted in CTI values of around 10^-7 or less. Some of the ten devices on the AXAF CCD focal plane will be back illuminated for enhanced detectivity below 1000 eV, and the process by which such devices are made and their performance has been described. Quantum efficiency values of about 0.7 have been obtained with such devices at carbon Kα X-rays (277 eV).

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