After the chip was placed onto the new TEC it has developed few blobs with increased dark current. We made an attempt to determine where the source of this dark is located, here are some results of the analysis. Three voltage scans were made at -70 C, voltage swing was maintained constant in each of them. 40 frames were acquired for each set of voltages, with frame integration time of 8 seconds. Scan # 1: Swing is 140 dac (about 7 Volts), negative dac goes from 140 (approximately -7 V) to 0 with the step of 10. Two clocks are kept low during the integration (at the moment I cannot tell which ones, need to hear from Steve).

Scan # 2: Same as the above, except that 2 clocks are kept high during the integration.

Scan # 3: Swing is 270 dac (about 15 Volts), negative dac goes from 160 (-8 Volts) to 40 (-2 Volts), 2 clocks were high during the integration.

After each scan was completed, Bev repeated a few points of the scan, moving in the opposite direction in order to see if the results are reproducible. In all cases, these additional points reproduced previous result very well. This can be seen in the Figures 1, 4, 7.

For the scan 1 the idea was to keep all gate voltages as negative as possible and see a transition from fully depleted operation to only partially depleted device. This seem to work the way we expected. Fig. 1 shows blob amplitude for each frame. The amplitude rises sharply as negative dac becomes smaller than 80. The amount of grade 7 events corresponding to the Mn $K_{\alpha}$ peak shows corresponding rapid increase at negative dacs higher than 90 (see Fig. 2). This would be consistent with the device becoming not fully depleted at low clock level more negative than -4 Volts. This voltage is not quite enough for inversion at the front surface of the device, so, most likely, this means that when there is no electric field at the back surface of the device, dark current drops significantly. Dark current in image area outside of the blob (Fig. 3) rises over slightly wider range, which is consistent with its origin at both surfaces.

Next 3 similar Figures are related to the scan #3 with large voltage swing. For this scan device is fully depleted at all voltages. The most negative dacs (corresponding to -8 V on the gate) were chosen to ensure that device goes into inversion at the front surface. Blob amplitude (Fig. 4) in this case rises gradually with rising electric field. Since there is no transition to undepleted state, it does not show sharp transition either. Inversion at the front surface does not seem to have a large effect, which, again is consistent with the blobs originating at the back surface. Number of grade 7 events is relatively small and changes with voltage (Fig. 5), but this change correlates very well with dark current (Fig. 6), with larger dark current and corresponding larger noise causing more grade 7 events. Dark current increase at very negative voltages must be caused by spurious charge onset (avalanche multiplication due to very large voltage swing) when the channel gets inverted at the front surface.
Figure 1: Scan 1, blob amplitude in each frame.

Figure 2: Scan 1, number of counts of grade 7 events corresponding to Mn $K_\alpha$ as a function of negative dac value.

While previous plots present a consistent picture of the blob current originating at the back surface, the last 3 figures related to the scan #2 (same swing as for #1, but two clocks high during
Figure 3: Scan 1, dark signal (image-overclock) as a function of negative dac value.

Figure 4: Scan 3, blob amplitude in each frame.

integration) present a puzzle that is not easily explainable (at least by me). The plot of blob current shown on Fig. 7 is similar to the plot for scan 1, except that transition to low current is shifted to more negative gate voltage. This makes sense because more gates are at positive voltage
Figure 5: Scan 3, number of counts of grade 7 events corresponding to Mn $K_\alpha$ as a function of negative dac value.

Figure 6: Scan 3, dark signal (difference between image and overlock) as a function of negative dac value.
than for scan 1. The problem arises, though, when one looks at the grade 7 plot at Fig. 8 that indicates that device is fully depleted for the entire scan, all voltages. Number of grade 7 counts in this case, similar to scan 3, is consistent with dark current values (Fig. 9) except for couple of anomalous points. But low and more or less constant number of grade 7 events means that there is no transition to undepleted bulk in this scan. It is not clear then what causes sharp rise in the blob current at negative dac 110. It can be inversion at the front surface, but corresponding voltage seems to be a bit too low for that. Besides, it is not in agreement with previous conclusion of the blob coming from the backside.

Figure 7: Scan 2, blob amplitude in each frame.
Figure 8: Scan 2, number of counts of grade 7 events corresponding to Mn $K_{\alpha}$ as a function of negative dac value.

Figure 9: Scan 2, dark signal (image-overclock) as a function of negative dac value.