Figure 7-2: APS-2 pixel layout. The four large rectangles make up the CDS capacitor $C_2$. The reset and source follower transistors use H-gates, while the current source and row-select switches use straight gates.

7.3 Simulation

APS-2 was simulated using the same bulk models used in Section 6.5.

Simulations suggest p-type transistors are leakier than n-type. Simply having zero gate-source voltage does not turn the transistor off enough to allow proper integration. It is possible that the edgeless H-gate designs solve this problem; SPICE does not have an easy way to account for gate shapes. Lowering the reset drain voltage allowed the simulation of the APS-2 pixel operating correctly. All simulations were done with the reset drain at 2.5 V, with the reset gate off voltage at 3.3 V. A 1 pF column capacitor was added to represent bus capacitance.

Basic operation

Despite the negative value of $V_{SG}$ used, simulations still showed the capacitive sense node being pulled up, without any photocurrent present, with a slope of 42 volts per second. This offset resulted in non-linear behavior when applying photocurrents of 100, 200, 500, and 1000 fA (Figure 7-3). Subtracting the offset, however, corrected for this deficiency, allowing linear operation of the APS-2 pixel (see Table 7.1). The gain, measured as output slope divided by input current, varies by 0.6% as photocurrent