

Charge Injection: Motivation

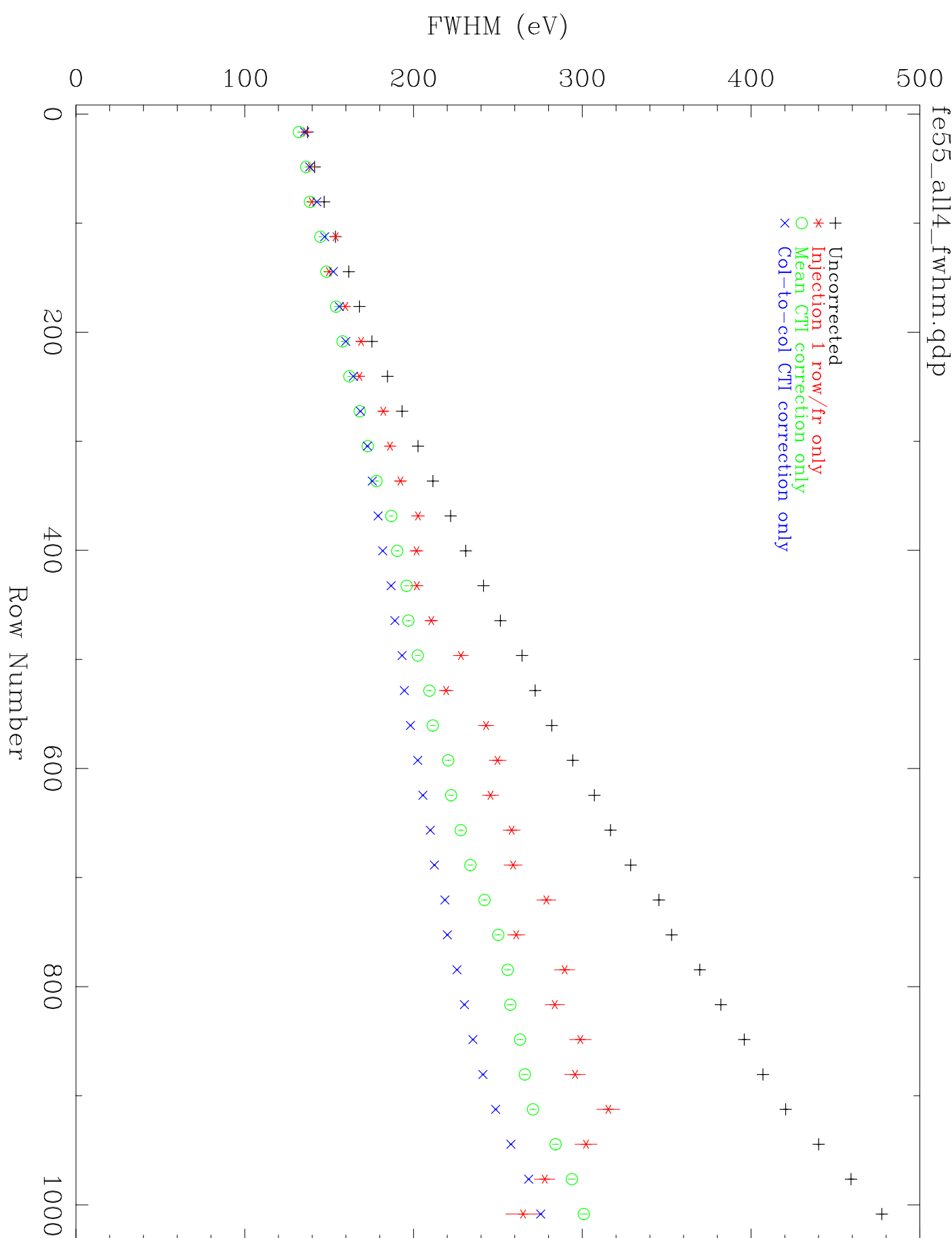
- **XIS performance late in Astro-E2 mission is especially important:**
 - * Science driven by XRS in first two years
 - * **XIS will be sole soft-X-ray instrument on Astro-E2 years 3-8**
- **Radiation-induced CTI increase for XIS will be comparable to SIS:**
 - * **SIS: $dCTI/dt \sim 3 \times 10^{-5} \text{ yr}^{-1}$** (Yamashita, Dotani et al. 1999 NIM-A 436 68)
 - * Lower XIS temperature makes modest ($\sim \times 2/3$) CTI improvement (for high energy protons!)
 - * Orbit and solar cycle phase similar to ASCA
 - * Shielding may be better for XIS, but XIS must transfer charge farther from aimpoint to readout (1.25 cm vs 1.0 cm)
- **Laboratory and flight tests show charge injection can significantly reduce effective CTI (by $\sim \times 3 - 5$)**
- **Charge injection may significantly improve XIS spectral resolution late in mission.**

ACIS Experience with Charge Injection and CTI Measurement

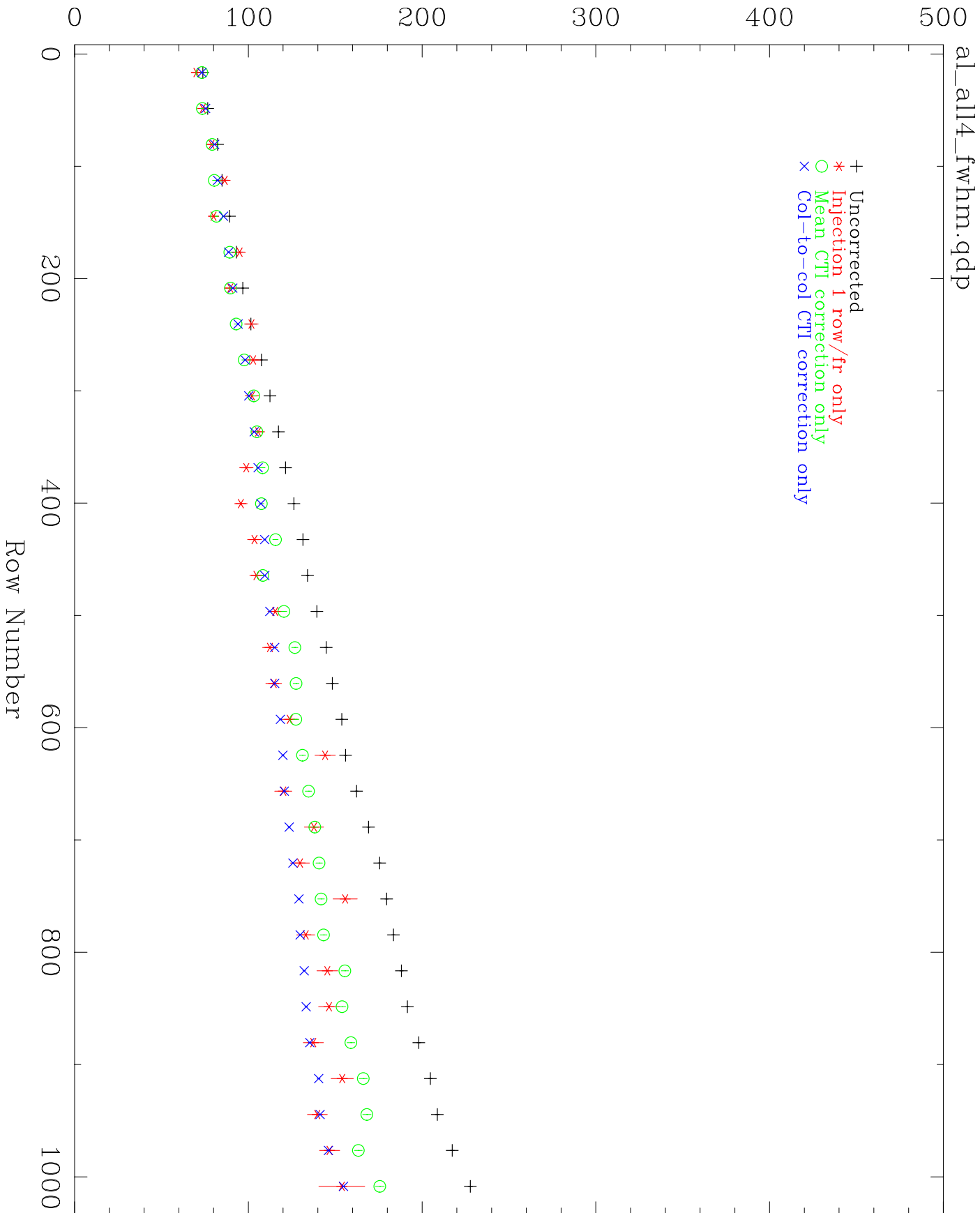
- Charge injection can help performance two ways:
 - * “Sacrificial charge” effect reduces CTI and improves resolution.
 - * Accurate measurement of CTI (vs. energy and position) allows ground correction and leads to better resolution.
- ACIS Squeegie experience (sacrificial charge effect):
 - * Inject one bright line ($> 10^4 e^-$ per 3.2s frame (T = -120C))
 - * Improves spectral resolution by $\times 1.7$ at 5.9 keV, by $\times 1.4$ at 1.5 keV.
 - * XIS results would probably not be this good with single injected line per frame, since XIS has higher detector temperature, longer frame time.
- ACIS experience with CTI measurement and ground correction:
 - * Charge loss varies significantly with charge-packet size ($\delta Q \sim Q^{0.53}$) so energy-dependent correction improves resolution for split events (helps high-energies most)
 - * CTI varies significantly with column (low-trap density statistical fluctuations) so column-by-column correction also helps.

FWHM with Charge Injection or CTI Correction ACIS at 5.9 keV

fe55_all4_fwhm.qdp

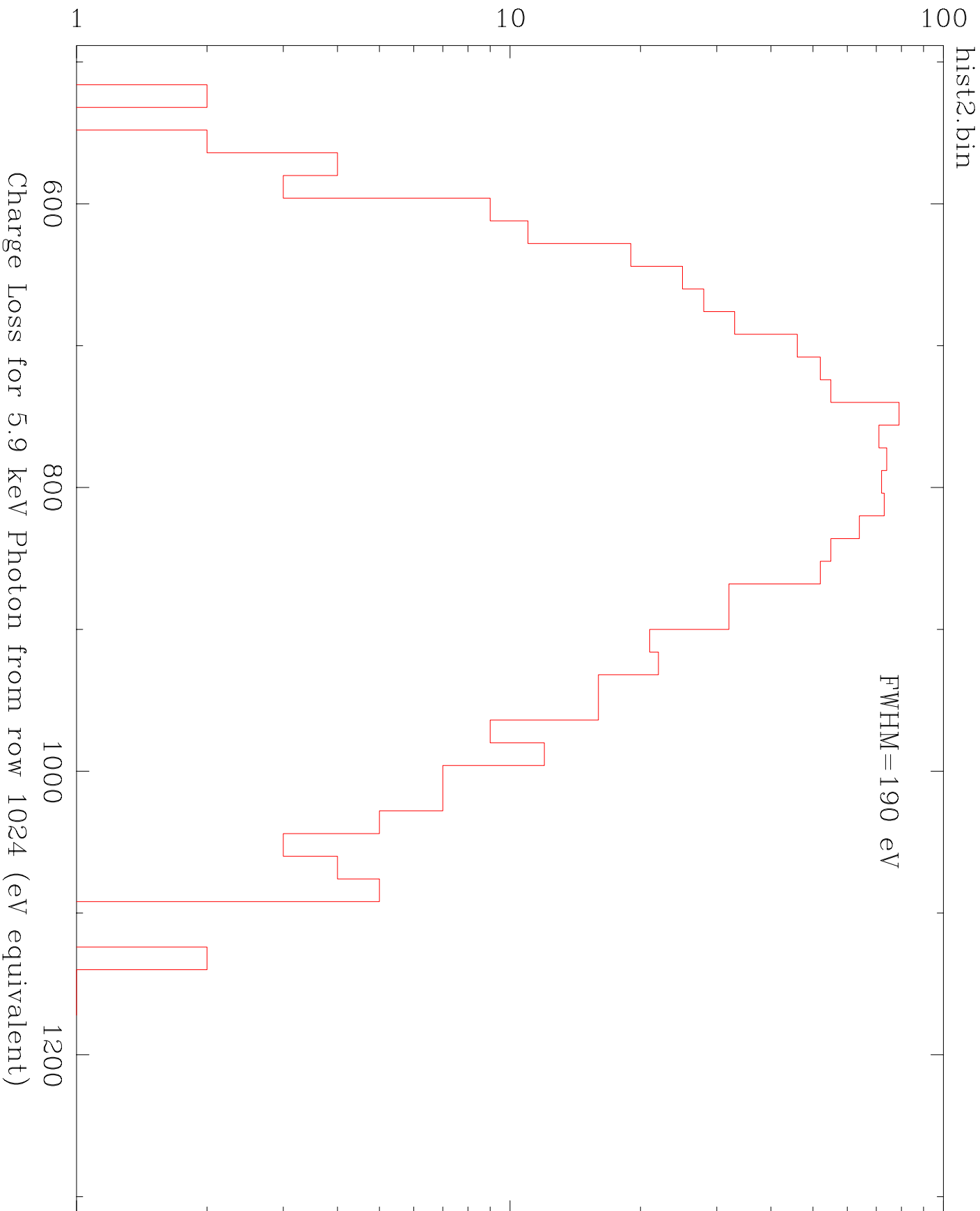


FWHM with Charge Injection or CTI Correction ACIS at 1.49 keV

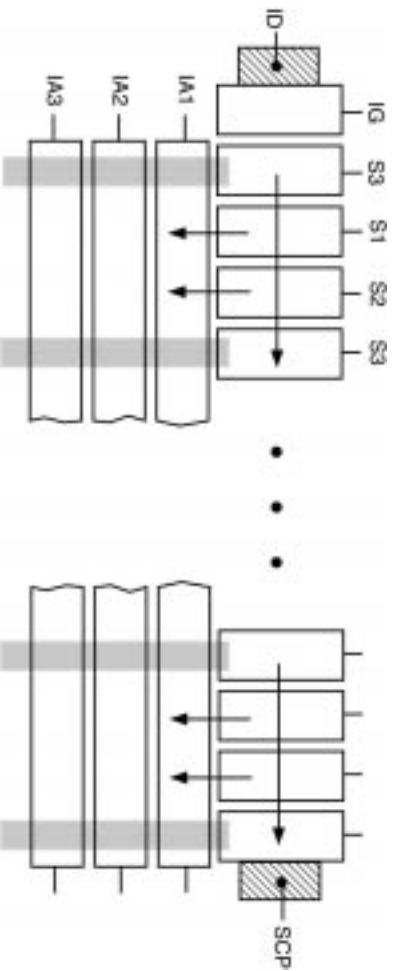


al_all4_fwhm.qdp

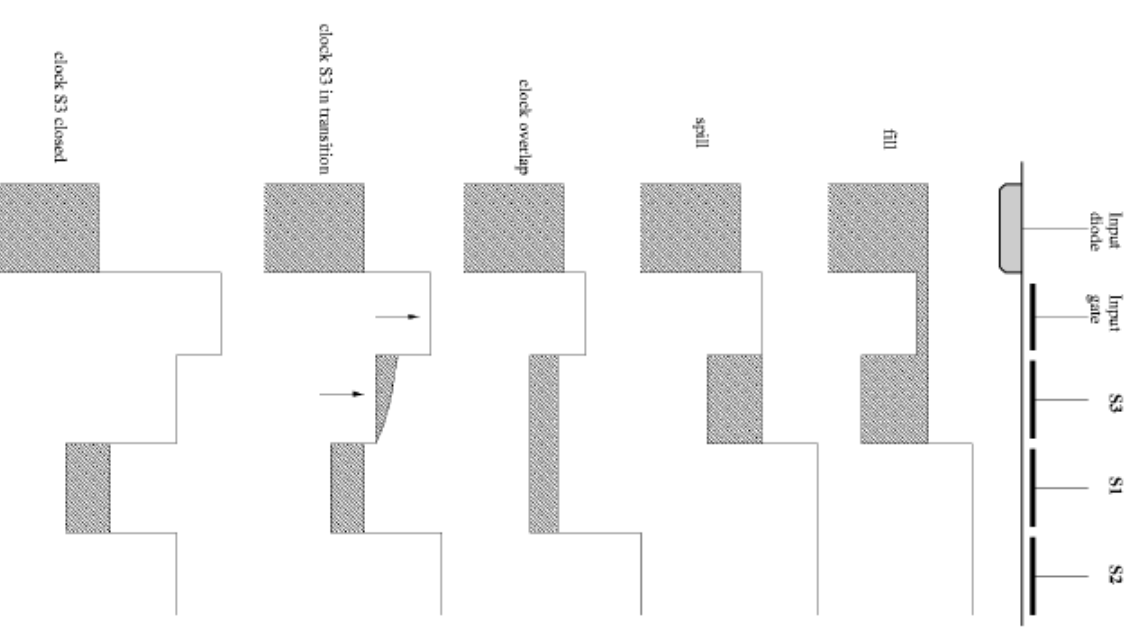
Column-to-column non-uniformity in ACIS FI Detector 13
5.9 keV



Proposed XIS Charge Injection Structure and Timing



- An input register is added “above” the imaging area (“row 1025”)
- During injection, input register is filled, pixel-by-pixel, from input diode, to create a line of charge which is then transferred through imaging area (IA)
- Adjustment of Input Gate (IG) to S3 potential allows precision control of quantity of injected charge:
 $\sigma_Q \sim 30 e^-$, RMS



Input register timing during injection

Charge Injection: Summary

- Flight and ground tests show charge injection can significantly reduce the spatial variation of the energy scale in radiation-damaged CCDs (effective CTI reduced by $\sim \times 3 - 5$)
- ACIS flight experience shows that accurate knowledge of CTI (*vs.* column and energy) allows improved energy resolution through ground correction.
- XIS does not have multi-energy calibration source illuminating entire detector.
- Hardware charge injection will significantly improve XIS spectral resolution and calibration accuracy in the post-XRS phase of AstroE2.
- Risks have been considered and found to be modest compared to those inherent in fabrication of new mask. Backup masks (without charge injection) are being fabricated.
- Required modifications to AE have been identified and are feasible.
- Detailed plans for calibration and use of charge injection remain to be determined.

Other XIS CCD Design Changes

- New XIS CCD is designated CCID41 (XIS-1 CCD was CCID17, as in ACIS.)
- Several changes will be made to accommodate current MIT Lincoln Lab design rules.
- These changes have each been demonstrated on at least one other MIT LL device.

Parameter	CCID17 (XIS-1)	CCID41 (XIS-2)	Remarks
Charge Injection Capability	S/W only	Input Register Available	
Channel Stop Width	4 μm	2 μm	Better low-energy QE Better high-energy QE
Gate Overlap	2 μm	1 μm	Better low-energy QE Lower capacitance
Undepleted Si	390 μm	540 μm	Larger dead-area Greater load on DE
“Scratch” Glass	1.0 μm PSG removed from IA	0.25 – 0.5 μm BPSG and 1.0 μm PSG removed from IA	BPSG provides better yield. Will use same etch as on XIS-1 to remove BPSG and PSG from IA

Science Impact of BPSG

- Current plan (revised since 12/01 SWG) is to remove entire BPSG layer from imaging area.
- Therefore BPSG should have no effect on XIS-2 detection efficiency.
- BPSG will be removed from imaging area using same process used to remove PSG from imaging area of XIS-1 detectors.

XIS CCD Backup Plan

- **Two CCD production lots are planned.**
- **Lot 2 production will not begin until performance has been verified at CSR through tests of a sample of Lot-1 devices.**
- **If unforeseen problems with the charge-injection structure compromise performance of Lot-1 devices, these structures can be omitted from Lot-2 devices with a simple change in production sequence; all necessary masks exist.**
- **Decision is required on Lot-2 CCD configuration by 15 October 2002.**
- **If all flight devices had to be obtained from Lot 2, XIS sensors could still be delivered in September, 2003.**

AE/TCE Electronic Parts Availability

- All parts required for flight complement of AE/TCE hardware (2 units plus spare boards) are either in-house at MIT or readily available.
- XIS-1 parts list was reviewed in 2001 and 4 potentially obsolete integrated circuits (of 24 used) were identified.
- Sufficient quantities of these parts either were found in MIT CSR inventory or have been procured through specialty distributors.
- Two IC substitutions for XIS-2: CA3080A for CA3080A3; REF43FZ for REF43BZ. Substitute parts qualified for full military temperature range.

CCD Production Status

- CCID41 production Lot 1 is on schedule for delivery of first devices to MIT CSR in August:
 - * 224 of 284 production operations completed as of 14 June 2002.
 - * Mean (high-priority) processing rate at fabrication facility is 60 operations/month. *XIS* has high priority.
- First wafer-level electrical test results expected in July.