XIS Activities at MIT

Mark Bautz, Steve Kissel & Rick Foster

Overview:

- CCD performance & status
- Sensor base status
- AE/TCE status
- Prospects for back-illumination

CCD Performance & Status

- CCD Inventory and Test
- CTI vs chip location on wafer
- Quantum Efficiency and Spectral Resolution
- Cosmetics: hot pixels & bad columns
- Edge glow summary (no news)
- Charge injection
- Radiation test results

CCD Inventory: Packaged Devices at CSR

- 13 packaged devices delivered to date
- 9 devices in flight packages, from 3 wafers:
  - 3 from wafer 1 (~250 nm BPSG):
    - 2 for sensor base engineering tests (c5,c9)
    - 1 for edge- etch demonstration (c3)
  - 1 from wafer 6 (~130 nm BPSG):
    - full calibration, then used for radiation test (c1)
  - 5 from wafer 4 (50-75 nm BPSG):
    - 4 “flight candidates” (c3, c5, c6, c7; 2.5 calibrated to date)
    - 1 damaged during packaging (c4)

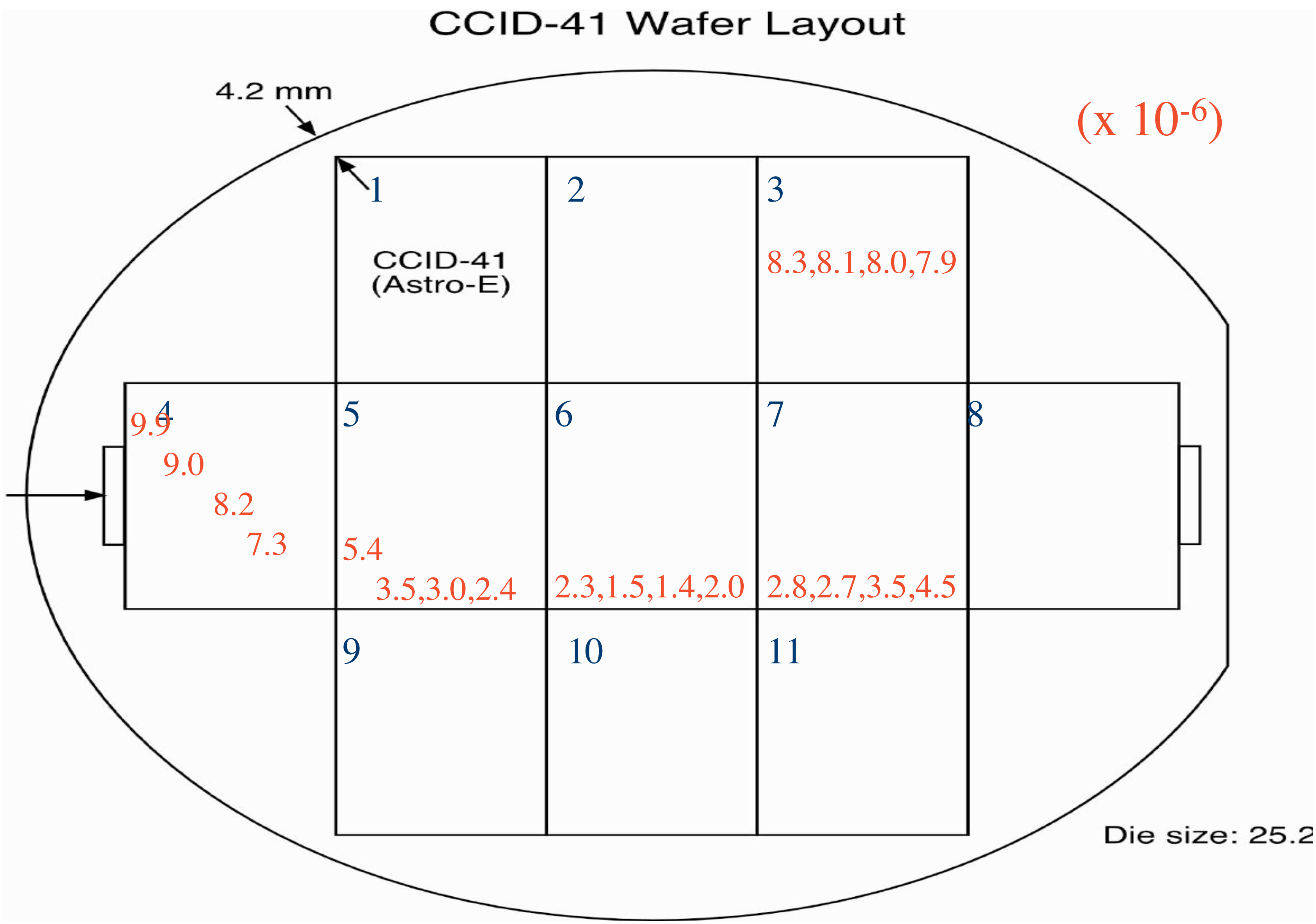
AstroE-2 XIS CCD Log

Device Number	Date Received	Drybox Log Page	Remarks
w1.1c4	24 July 2002	1	72-pin package; wafer 1.1 has ~ 0.2μm BPSG remaining. Quad C dead. Trouble with CI. Returned to LL 5 Aug 02
w1.1c11	5 Aug 02	2	"Flight-like" package, but with thin ceramic. Used for 1st succesful CI testing 2 Oct02. Returned to LL for CI tets there 4 Oct 02
w1.6c11	22 Aug 02	3	Thin ceramic, non-flight flexprint, only quad A works. NOT FLIGHT. 9 sep 02 back to LL for repair. 23 sep 02 back to CSR, no CI cap. on flexprint quads A &C work 26 sep 02 back to LL by mistake 30 sep 02 back at CSR.
w1.6c1	23 Sep 02	4	Full flight-like package, 70nm BPSG; flight candidate
w1.10c11	29 Oct 02	5	No charge injection; non-flight kovar package
w1.4c5	19 Nov 02	6	Flight candidate; wafer 4 is nominally overthinned to -30nm BPSG; RG short (solder on flex) repaired at LL
w1.4c6	22 Nov 02	7	Flight candidate; wafer 4 is nominally overthinned to -30nm BPSG. Edge glow 2Jan03;rtn to LL 8Jan03
w1.1c5	22 Nov 02	8	Engineering device for heatsink qualification. NB: wafer 1 has thick BPSG
w1.4c3	16 Dec 02	9	Flight candidate; wafer 4 is nominally overthinned to -30nm BPSG
w1.4c4	23 Dec 02	10	NON-FLIGHT: input register phase 2 shorted to ground, not bonded to flex; charge-injection not functional
w1.4c7	23 Dec 02	11	Flight candidate; wafer 4 is nominally overthinned to -30nm BPSG. rtn to LL to remove IG diodes 3Jan03; back from LL with no IG diodes 7Jan03
w1.1c3	25 Feb 03	12	Non-flight; edge-etched.
w1.1c9	27 Feb 03	13	Non-flight; replacement for qualification model sensor base.

CTI vs Chip Position

- XIS2 CTI is measurably higher than that of XIS1 devices:
  $2 - 10 \times 10^{-6}$ for XIS2 vs $< 3 \times 10^{-6}$ for XIS1
- Charge injection tests imply extra CTI due to very short-timescale trap (possibly Cu contamination?; cf Steve)
- Screening results indicate that CTI is best nearest the center of the wafer, and degrades systematically toward edge.
- On wafer 4, 3 central chips (5, 6 & 7) have CTI $< 5 \times 10^{-6}$
- We will attempt to choose flight devices from chip positions 5, 6 & 7.

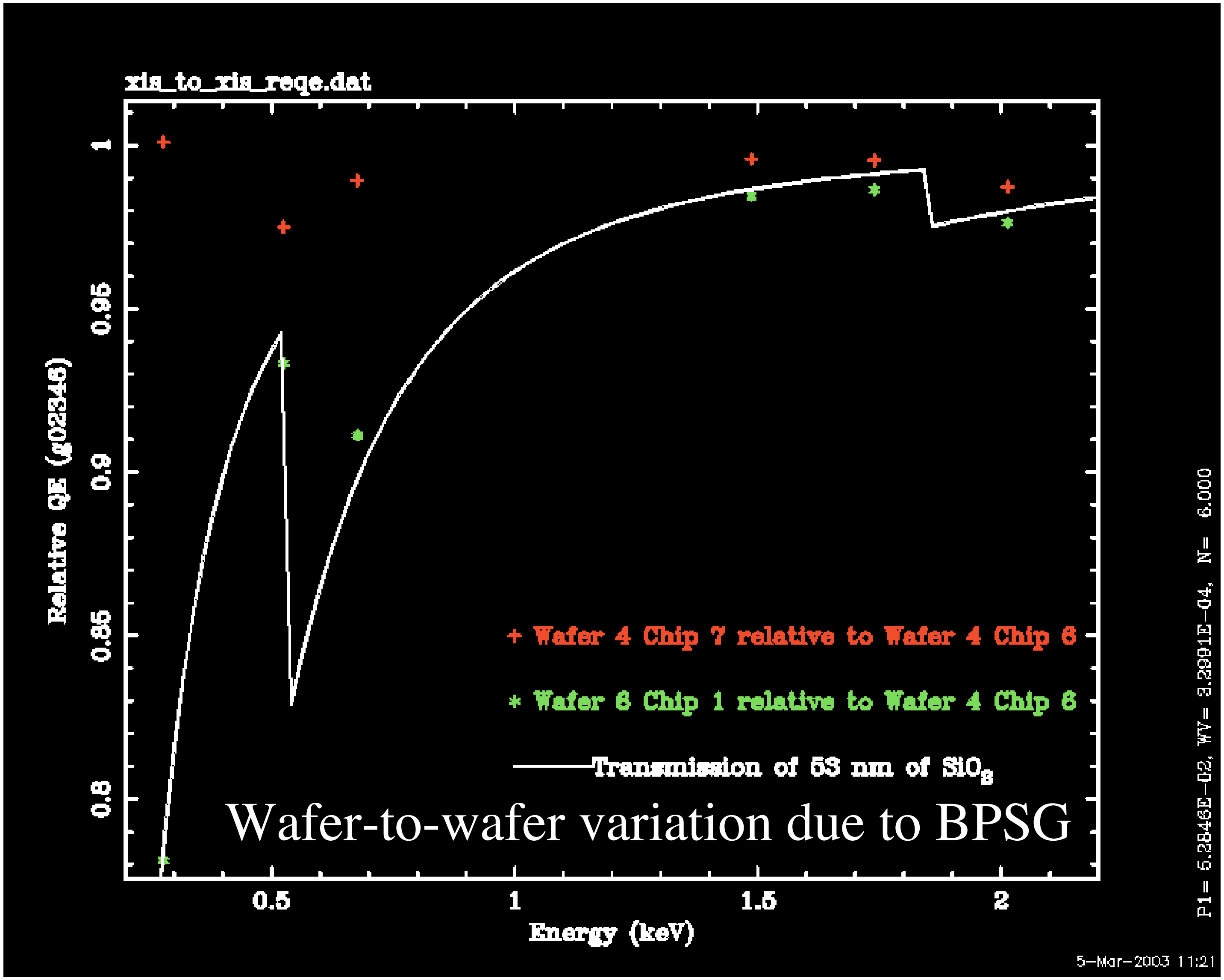
Wafer 4 CTI


CCID-41 Wafer Layout
(x 10^{-6})
4.2 mm
1
CCID-41 (Astro-E)
2
3
8.3,8.1,8.0,7.9
4
9.9
9.0
8.2
7.3
5
5.4
3.5,3.0,2.4
6
2.3,1.5,1.4,2.0
7
2.8,2.7,3.5,4.5
8
9
10
11
Die size: 25.2

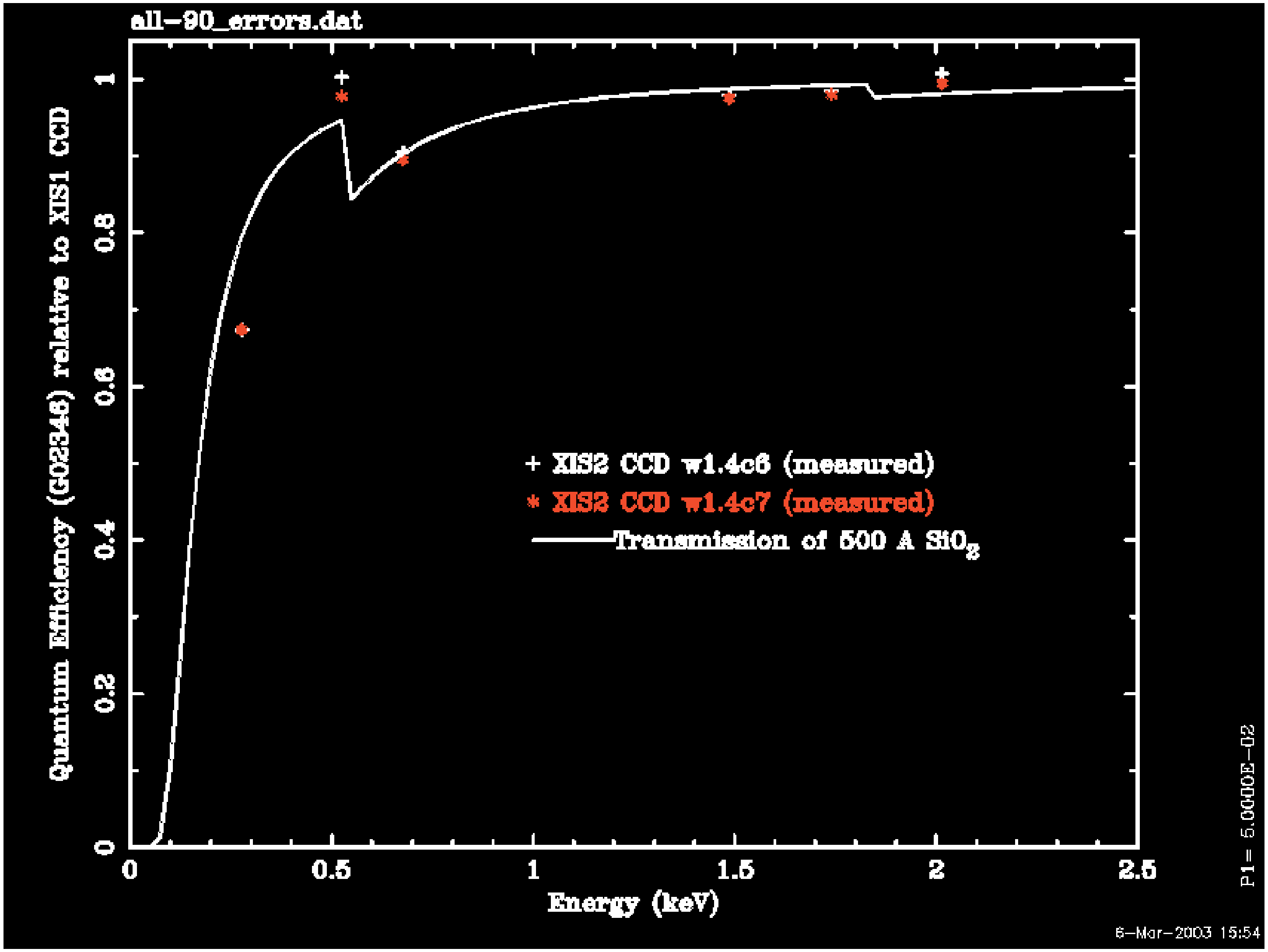
Quantum Efficiency

- QE measured for 1 w6 and 2 w4 devices (3rd w4 in now being measured)
- QE is as expected
- BPSG is main change from XIS1
- Final BPSG thickness is 50-75 nm
- Depeletion Depth ~ 65 □m, same as XIS1

Relative QE: XIS2 vs XIS2

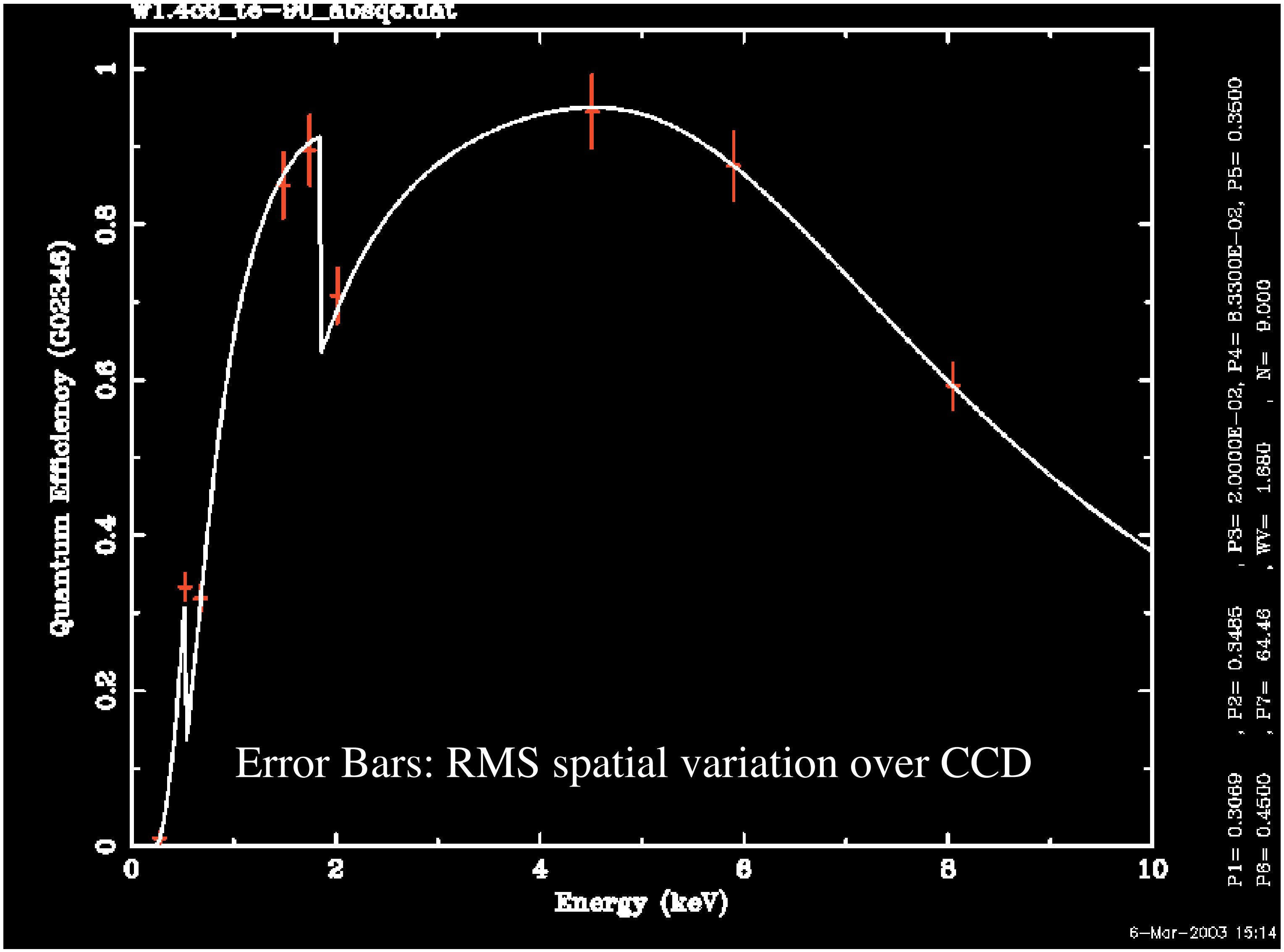


Relative QE: XIS2 vs XIS1

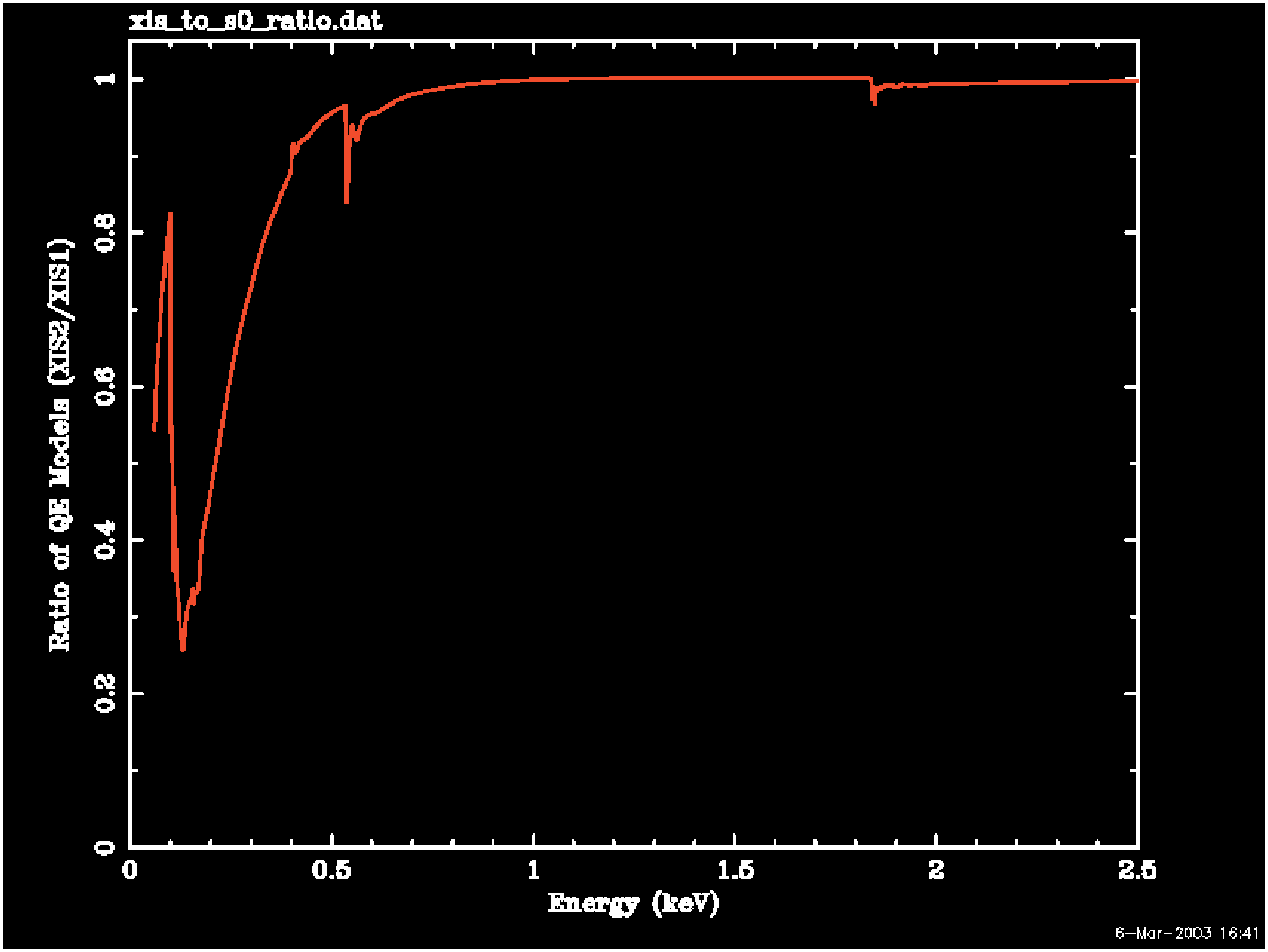


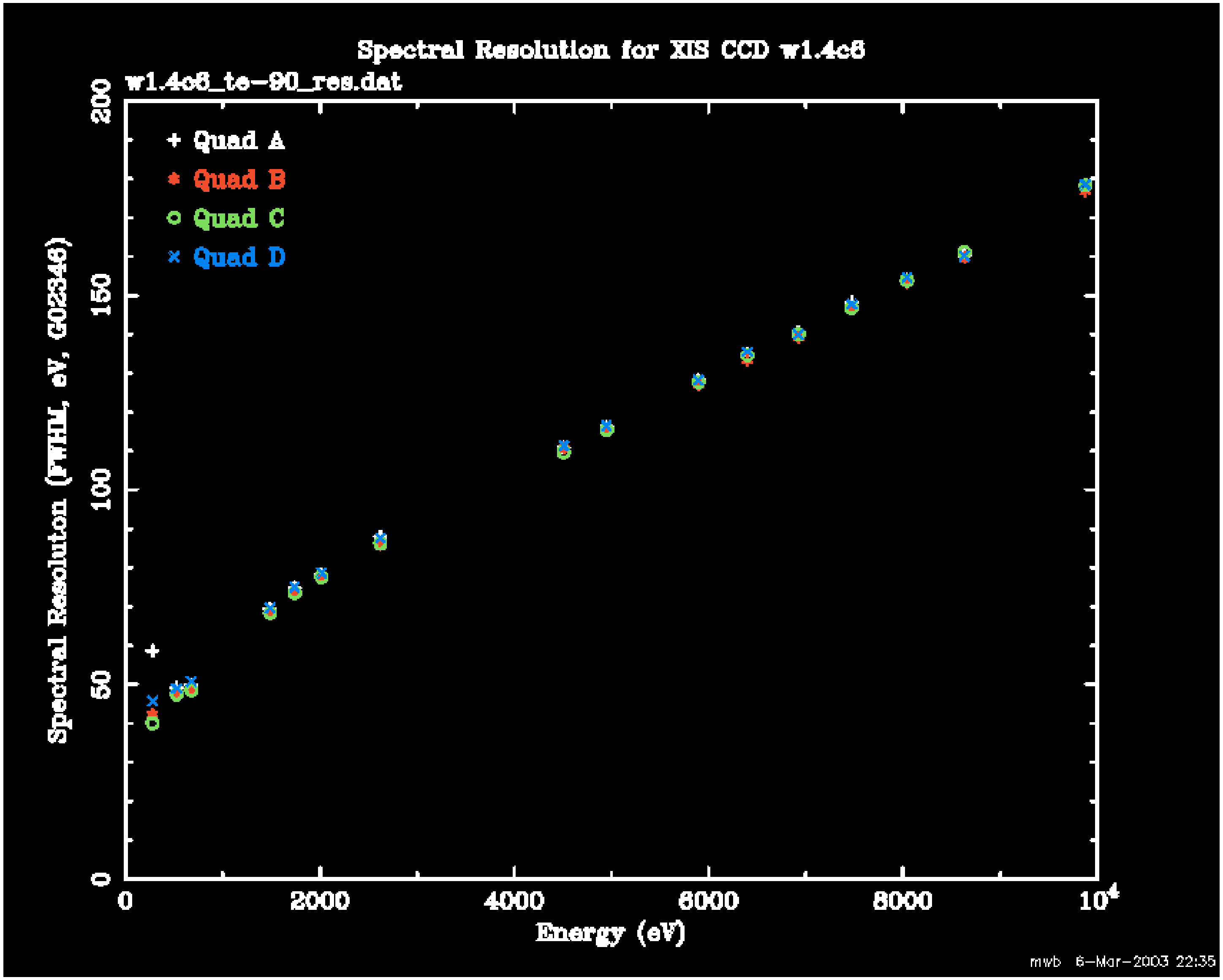
XIS2 CCD Absolute Quantum Efficiency

Measurements & Model

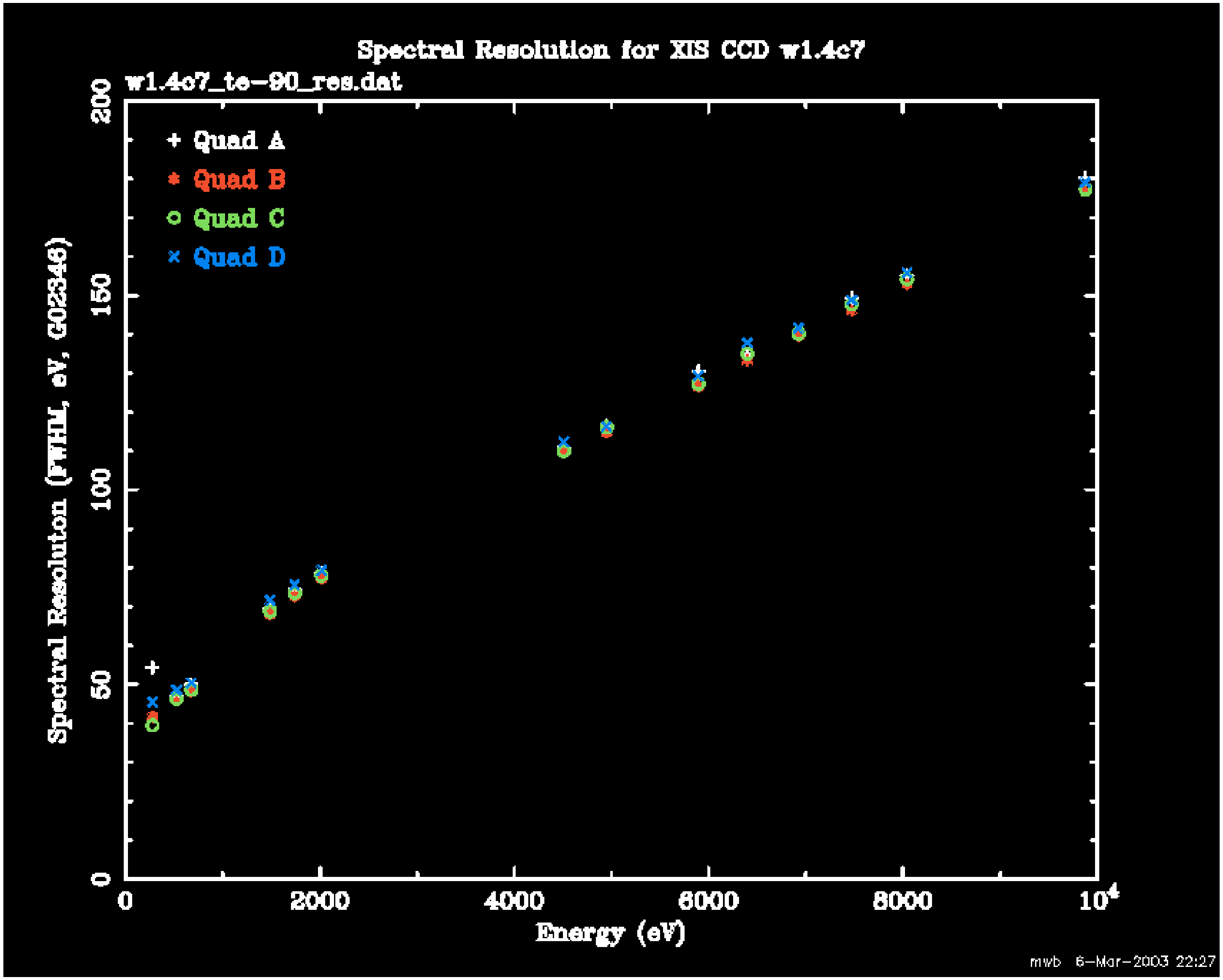


CCD QE Model Comparison: XIS2/XIS1





Spectral Resolution for XIS CCD w1.4c6
w1.4c6_te-90_res.dat
Spectral Resoluton (FWHM, eV, G02346)
Energy (eV)
+ Quad A
* Quad B
o Quad C
× Quad D
0
50
100
150
200
0
2000
4000
6000
8000
10^4
mwb 6-Mar-2003 22:35



Spectral Resolution for XIS CCD w1.4c7
w1.4c7_te-90_res.dat
+ Quad A
* Quad B
o Quad C
× Quad D
Spectral Resoluton (FWHM, eV, G02346)
0
50
100
150
200
0
2000
4000
6000
8000
10^4
Energy (eV)
mwb 6-Mar-2003 22:27

Hot Pixels & Bad Columns

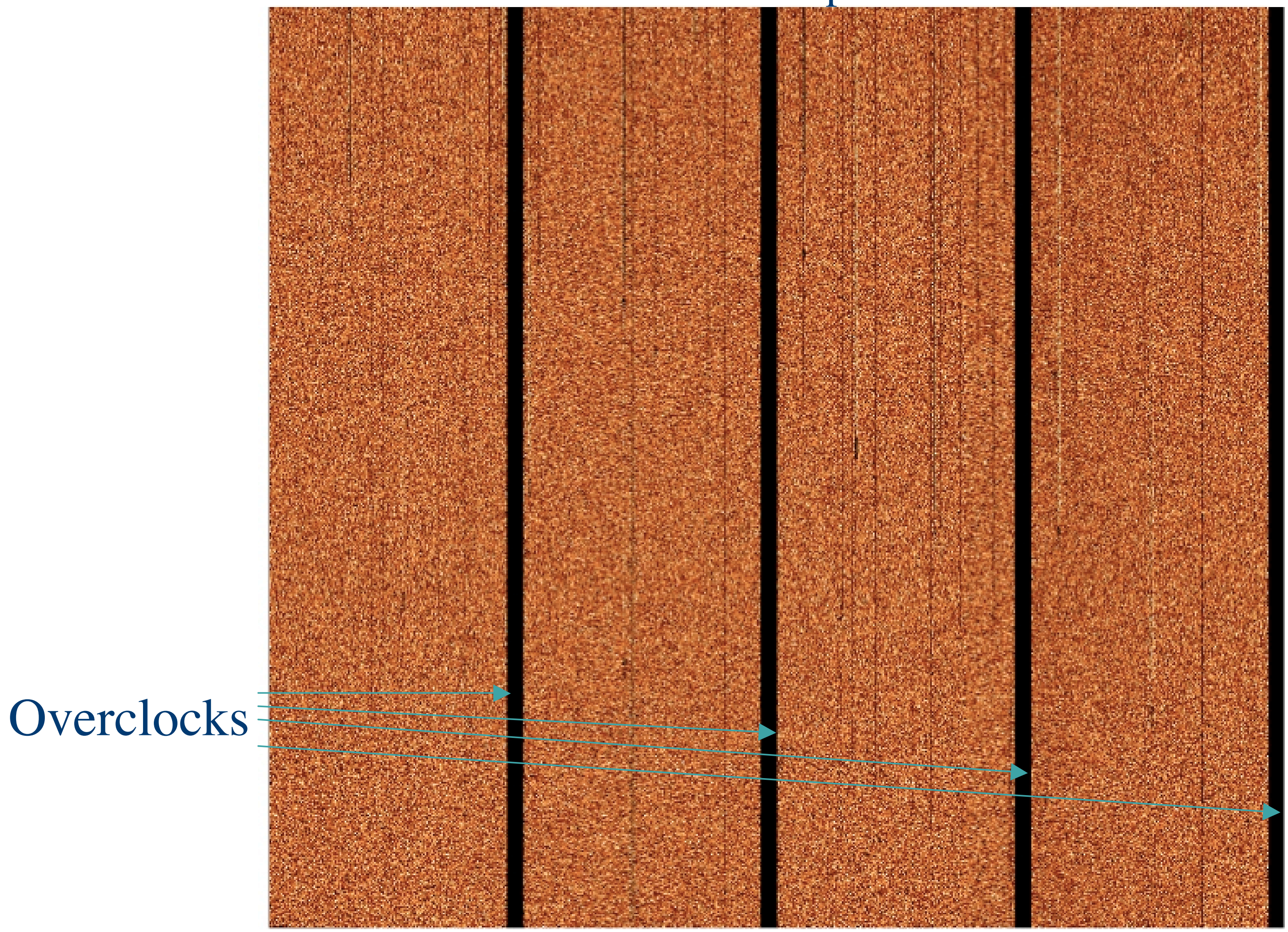
- XIS2 devices show 35-75 “hot pixels” (fewer at T=-70C!)
- Each hot pixel produces ~ 1 event/readout:

Can DE &/or telemetry accommodate these?

- Typically ~ 50 “bad” columns; may be related to “hot pixels”
- Suggest Japanese side review raw data

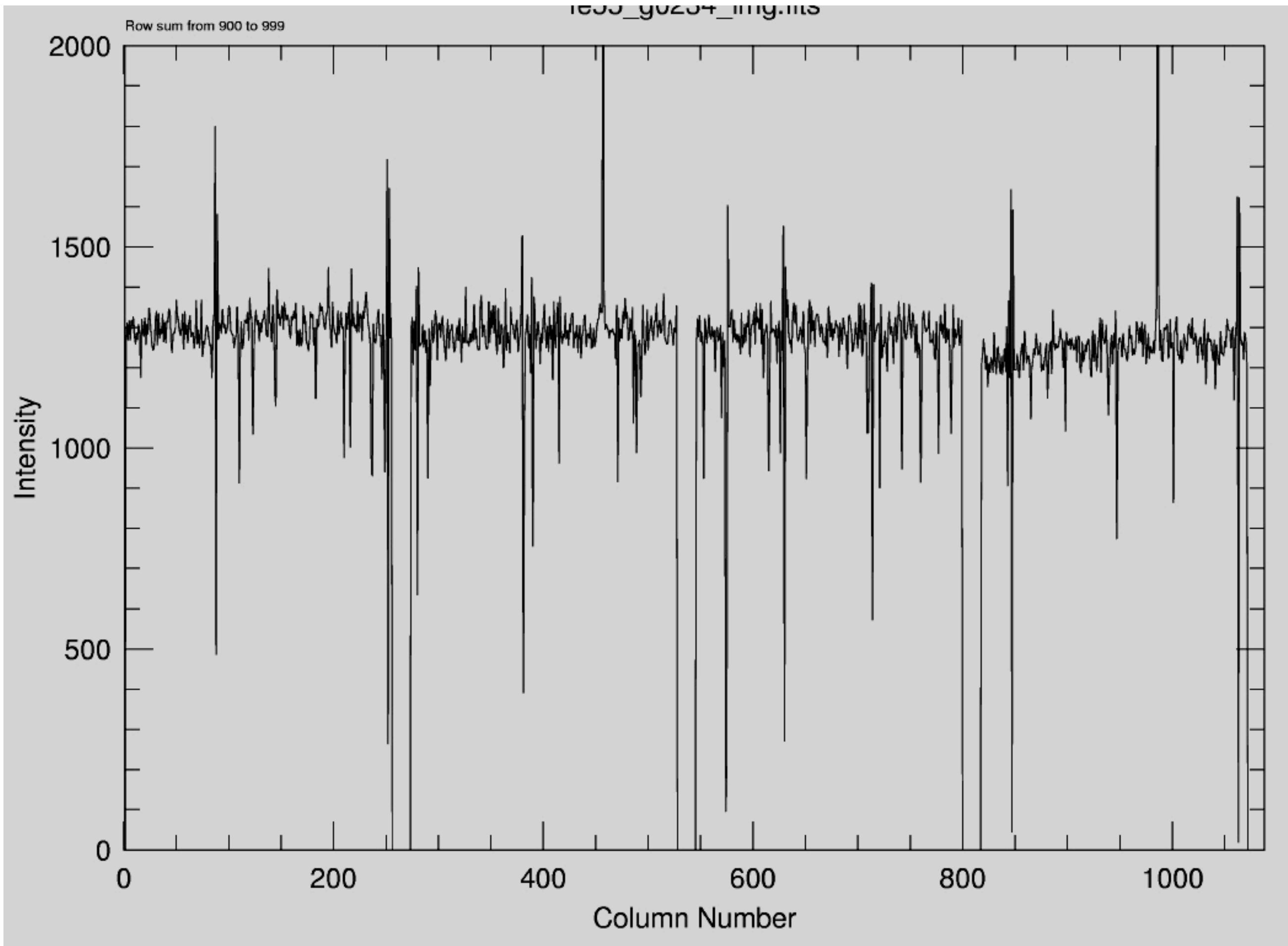
QE Non-uniformity of w1.4c7

10^7 5.9-keV photons

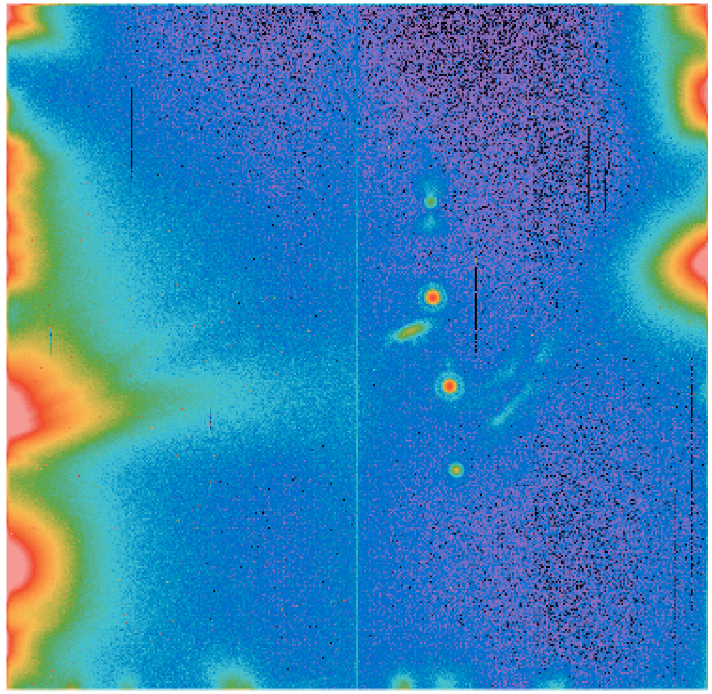


QE Non-uniformity in w1.4c7

Events/col in rows 900-999



Column Number



Recent Glow Example

Associated with following:

Specific vacuum chamber
Specific pump or foreline?
Anomalous vent precedes glow
Ambient conditions remove glow
Glow only Jan. 2003 ?

Glow amplitude sensitive to BJ voltage

Insensitive to following:

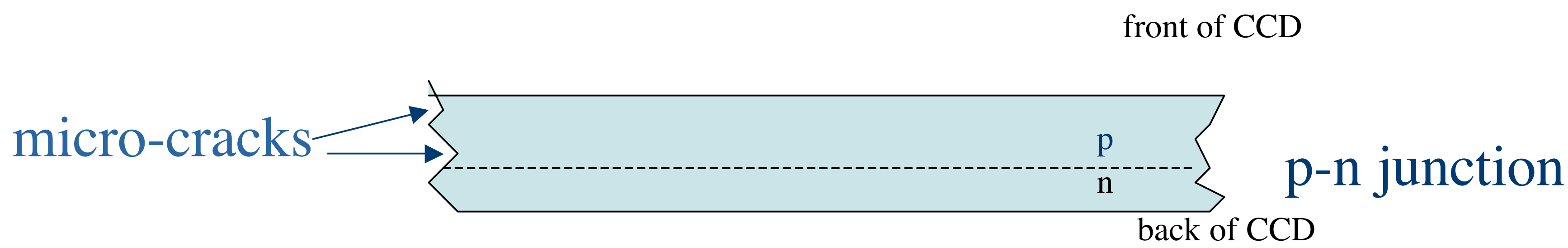
CCD Type (ccid17, ccid41)
Electronics (ACIS-DEA, XIS)
Readout method
Temperature
Presence of x-rays, other sources
Ambient vacuum conditions
Power cycling

Unable to produce glow on demand

Response to Edge Glow

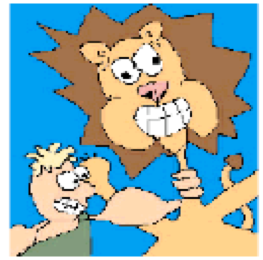
- Have NOT identified cause of intermittent edge glow, but glow is probably related to saw damage.
- Have demonstrated edge-etching, originally developed for ASCA, on XIS2 CCD.
- Will package & calibrate at least 4 additional devices (from wafer 7) for use in flight sensors.
- Propose to fly only edge-etched devices.
- First edge-etched, wafer 7 device expected at CSR this week.

Putative Edge-glow Mechanism



- Back-junction is a reverse-biased diode
- Function is to remove charge from "deep" background events
- Micro-cracks on edge of chip (from sawing) near p-n junction can produce (locally) high electric fields.
- High fields lead to impact ionization & large numbers of electrons-hole pairs.
- Some of these electron-hole pairs recombine & emit near-IR photons which are "detected" as edge-glow.
- Etching edges removes or reduces curvature in micro-cracks.

Charge Injection Implementation



猫の皮をむく方法はたくさんが あります

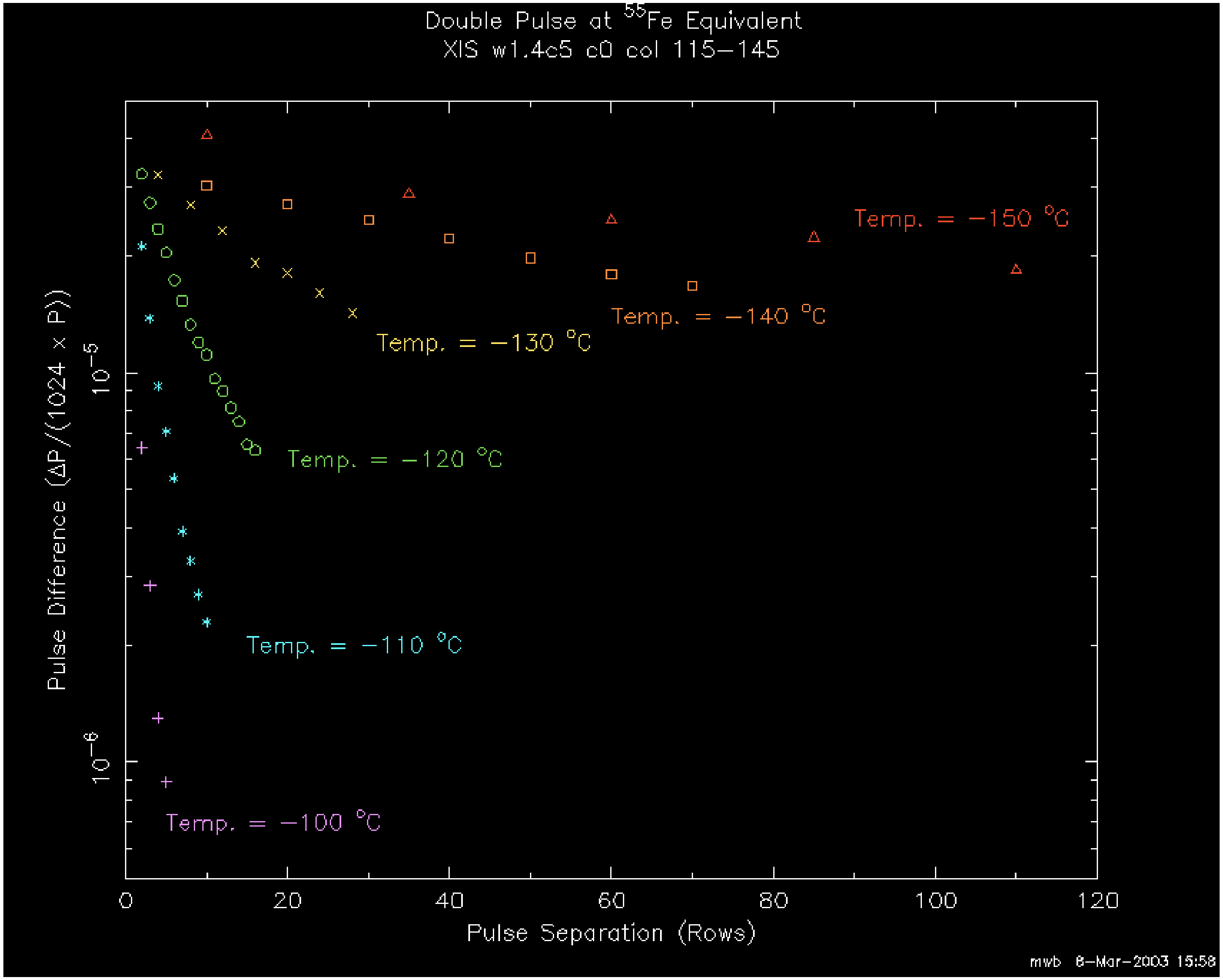
<u>Pixel Pattern Generation Method:</u>
- Current Default implementation
- ON/OFF By Command
- Output migrates with event list

<u>Double Pulse Experiment:</u>
- Technique for identifying traps
- Not easily implemented

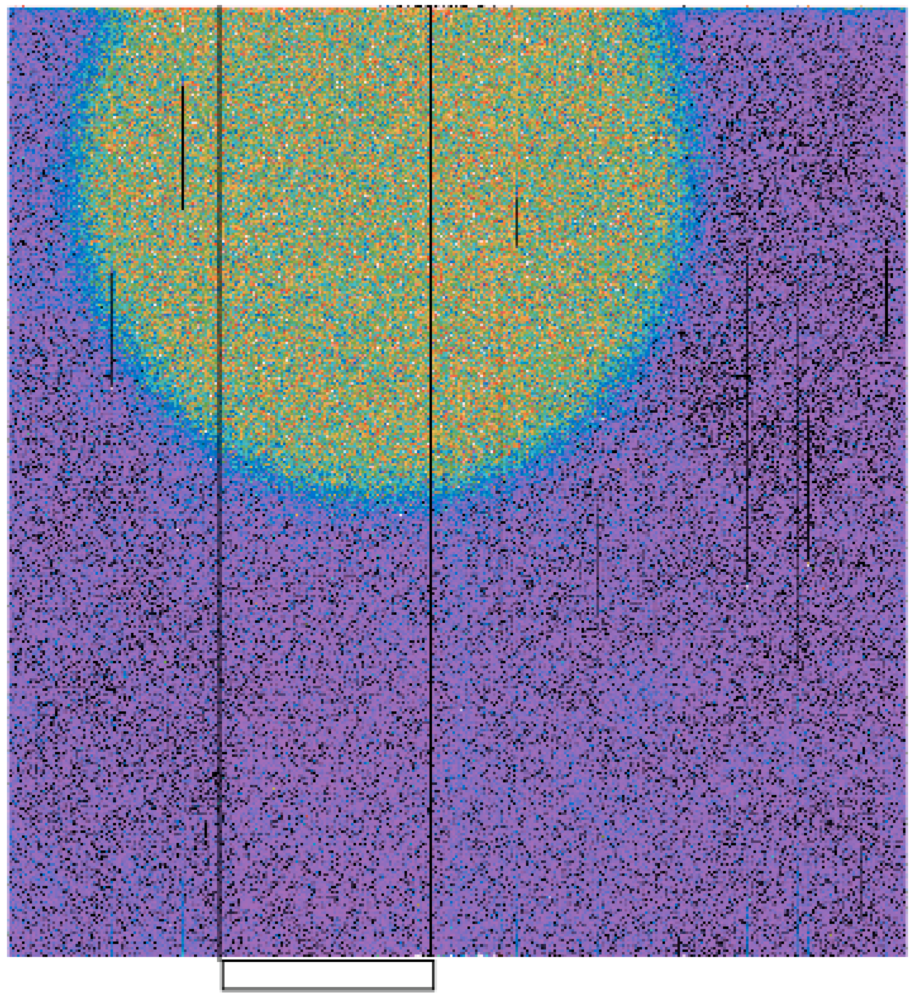
<u>Row Grid Experiment:</u>
- Example of possible flight model
- Easy implementation, low impact

The 1st labor of Hercules was to slay the Nemedean Lion. He flayed the creature's inpenetrable skin using its own claws - thus the source of the expression "more than one way to skin a cat." The term persists to this day in a multitude of languages.

* No actual cats were harmed in the course of these experiments.

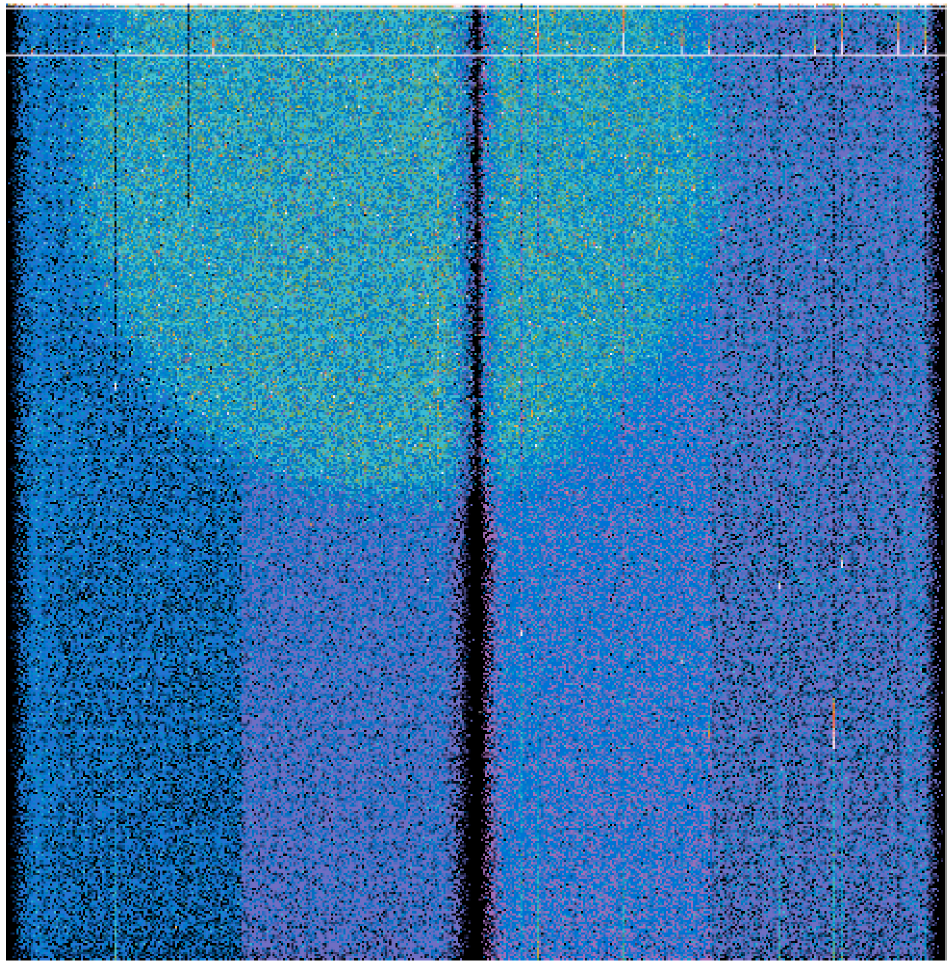

Double Pulse at 55Fe Equivalent
XIS w1.4c5 c0 col 115–145
Pulse Difference (ΔP/(1024 x P))
10−5
10−6
Temp. = −150 °C
Temp. = −140 °C
Temp. = −130 °C
Temp. = −120 °C
Temp. = −110 °C
Temp. = −100 °C
0
20
40
60
80
100
120
Pulse Separation (Rows)
mwb 8-Mar-2003 15:58

40 MeV Proton Irradiation Pattern

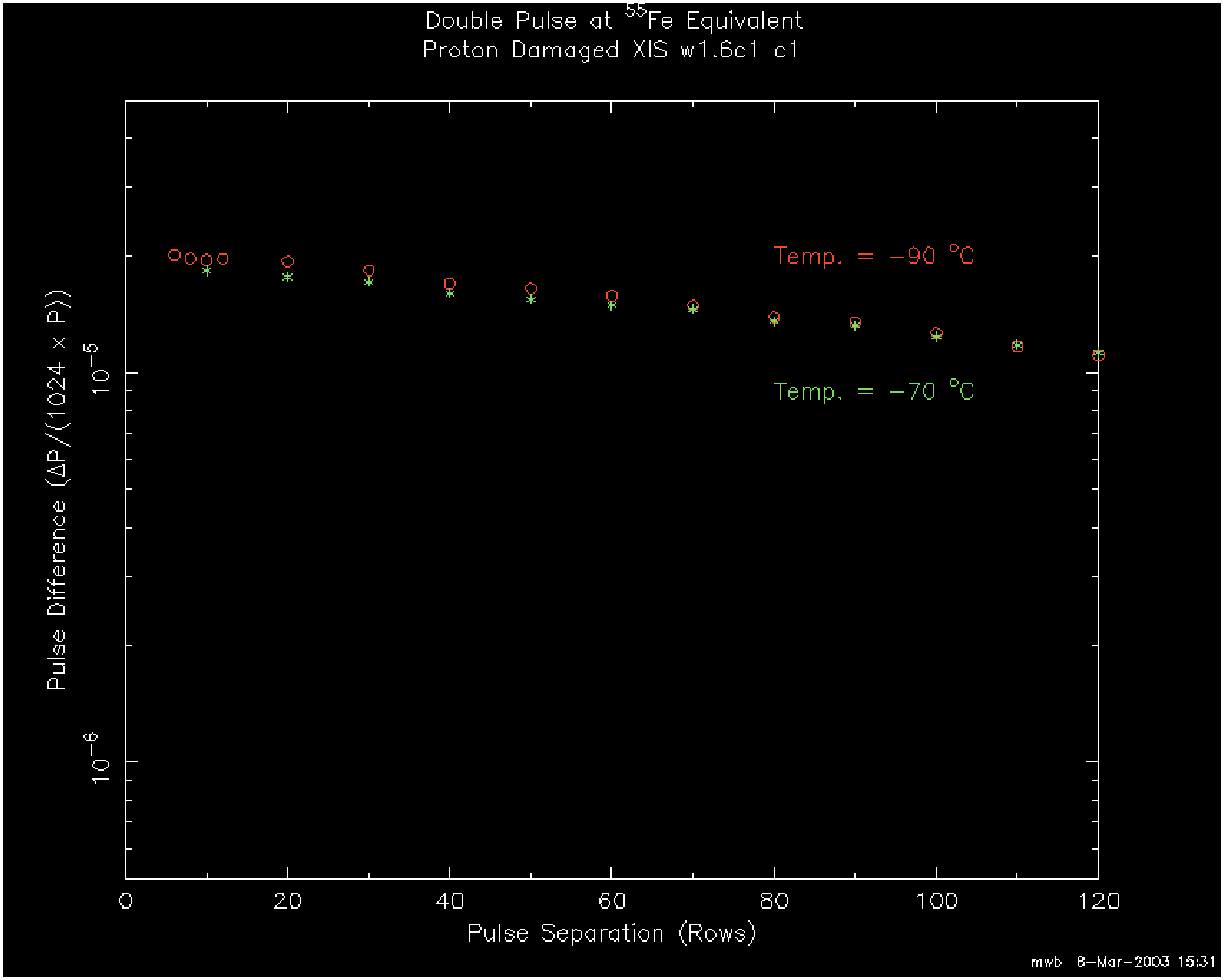


Output B (c1) used for comparison

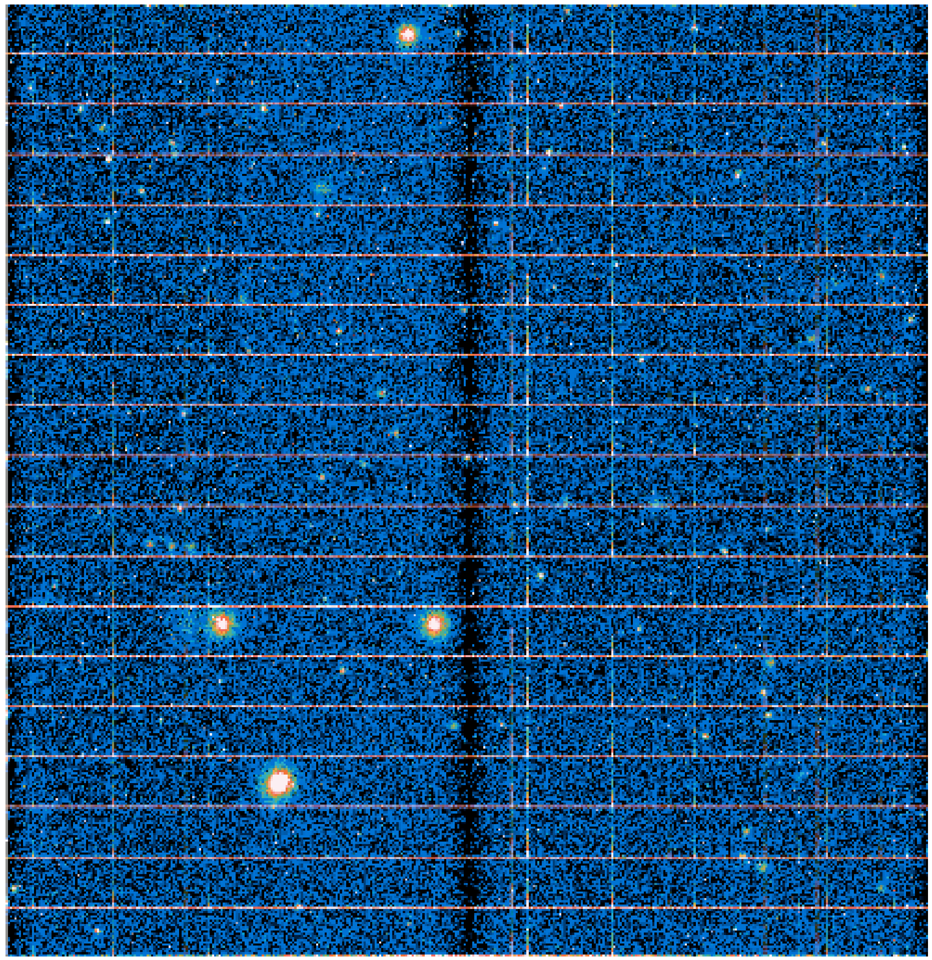
XIS Charge Injection
Double Pulse Experiment



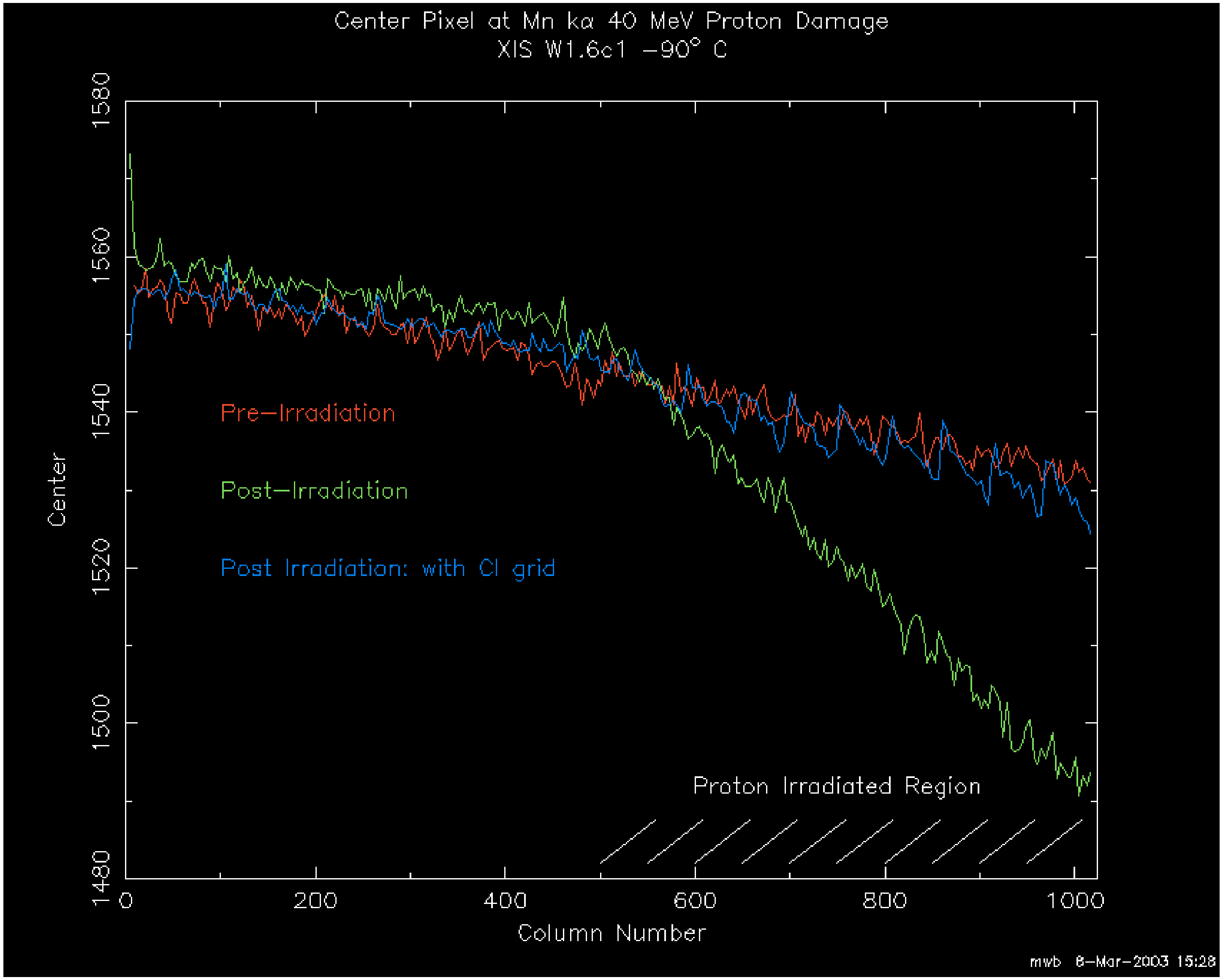
2 rows of charge are placed in the image array prior to integration and readout. The amplitude of the second row may be increased due to trap filling by the leading row. This increase is measured versus row spacing (24 microsecond per row) and reveals the effective detrapping time(s).

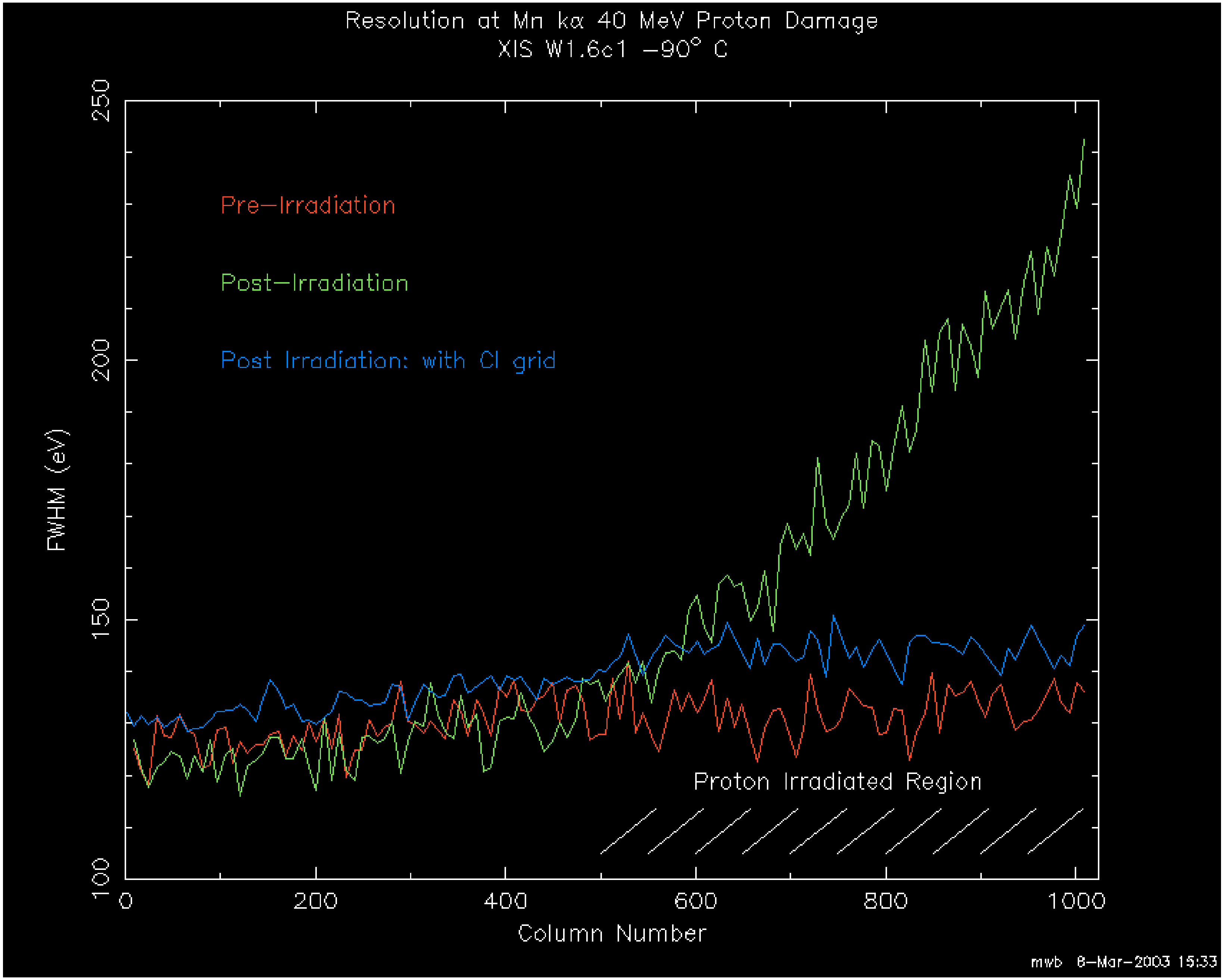

Double Pulse at 55Fe Equivalent
Proton Damaged XIS w1.6c1 c1
Temp. = −90 °C
Temp. = −70 °C
Pulse Difference (ΔP/(1024 x P))
10−5
10−6
0
20
40
60
80
100
120
Pulse Separation (Rows)
mwb 8-Mar-2003 15:31

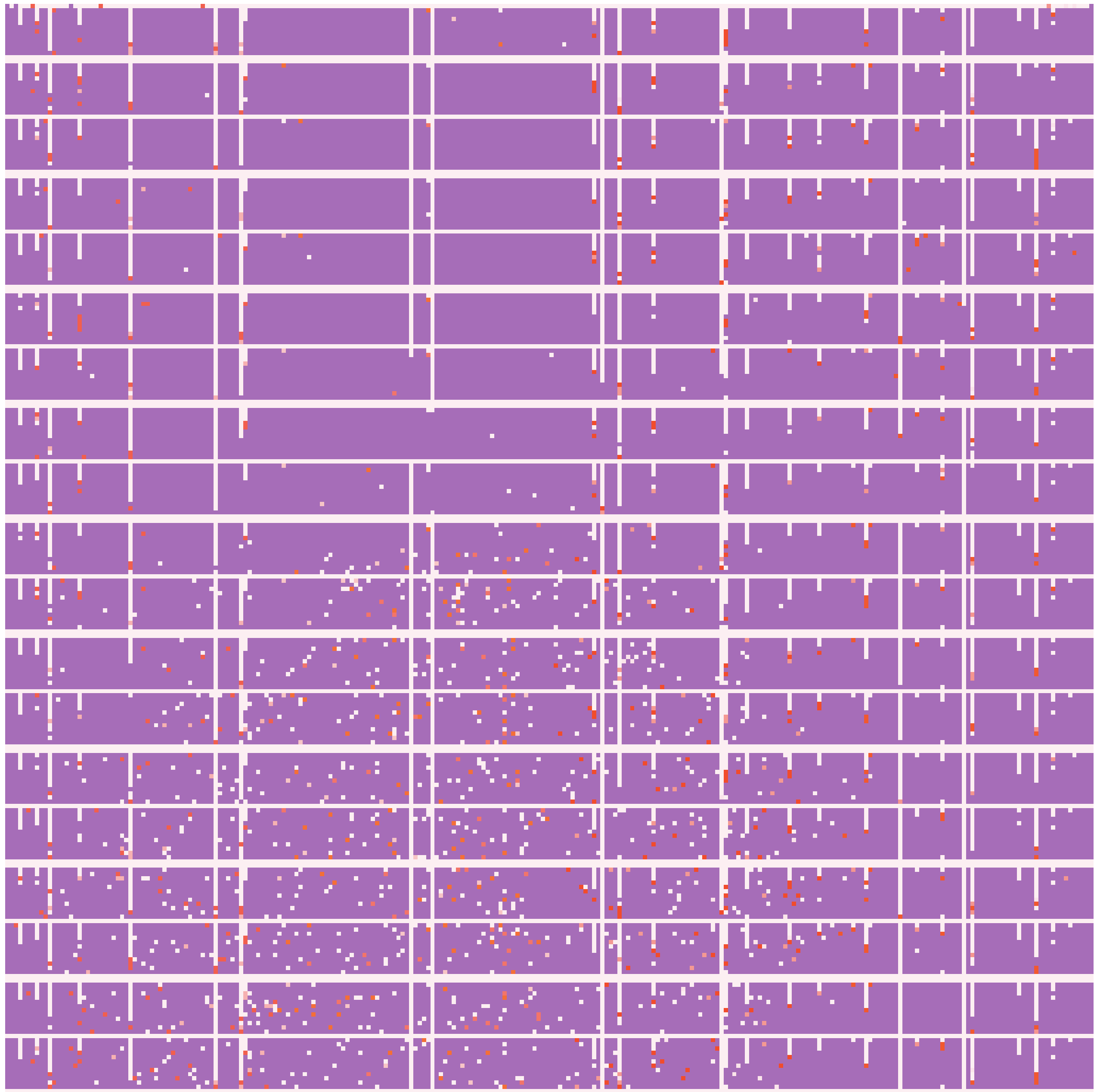
XIS Charge Injection
Row Grid Experiment



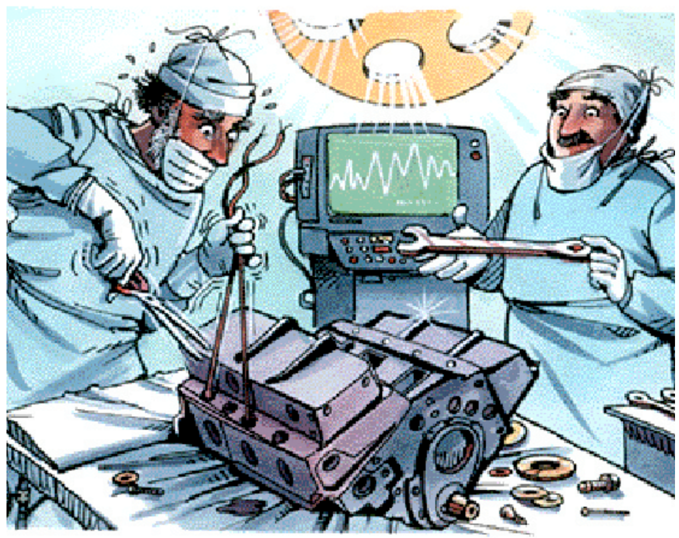
A grid of charge injected rows (spacing = 54) is placed in the image array prior to exposure and readout. The amplitude is larger than any expected x-ray charge packet.


Center Pixel at Mn kα 40 MeV Proton Damage
XIS W1.6c1 −90° C
Center
1480
1500
1520
1540
1560
1580
0
200
400
600
800
1000
Column Number
Pre−Irradiation
Post−Irradiation
Post Irradiation: with CI grid
Proton Irradiated Region
mwb 6−Mar−2003 15:28


Resolution at Mn kα 40 MeV Proton Damage
XIS W1.6c1 −90° C
FWHM (eV)
100
150
200
250
0
200
400
600
800
1000
Column Number
Pre−Irradiation
Post−Irradiation
Post Irradiation: with CI grid
Proton Irradiated Region
mwb 8−Mar−2003 15:33



AstroE2 XIS Engineering Status



AstroE2 Science Working Group Meeting

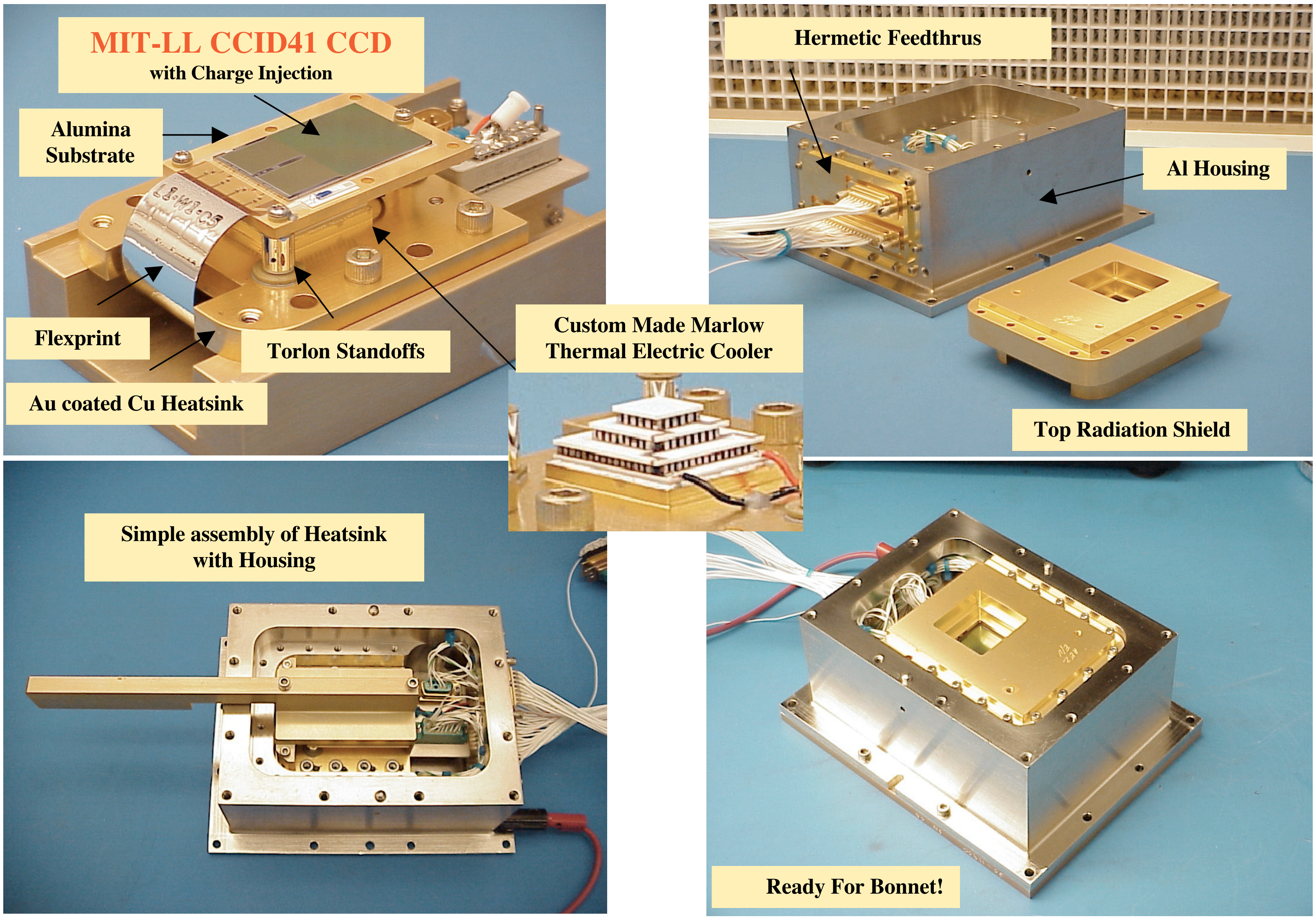
March 2003

ISAS

Topics

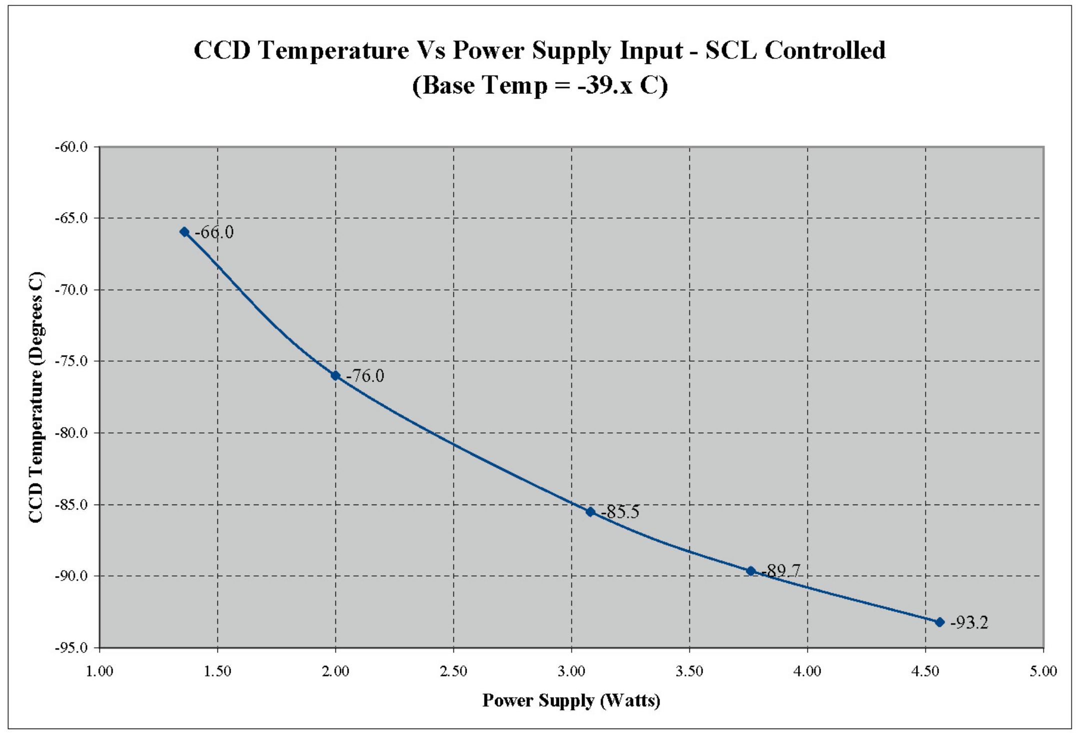
- Sensor Base
  - Heatsink Assembly Redesign
    - Design Overview
    - Thermal Performance Test Results
    - Torlon standoff delamination issue
  - Sensor Base
- Analog and Thermal Control Electronics
  - Electrical
  - Mechanical
  - Software/Firmware
- Programmatics
  - Schedule

XIS Sensor Base Qualification Model



Sensor Base

- Engineering Unit Thermal Performance
  - Initial Thermal Performance Tests of Sensor Base with the redesigned heatsink showed excellent results.
  - Noticeable improvement over AstroE1 performance



Sensor Base (Cont.)

- Torlon Standoff Configuration
  - The CCD is held in position with 3 Torlon posts bonded to a copper heatsink
  - The torlon provides structural support for the CCD and has very good thermal isolation properties
  - The adhesive bondline (Hysol EA 9394) between the bottom of the torlon standoffs and the heatsink is used to take up the machine tolerances of the standoffs and the thermal electric cooler (which is sandwiched between the CCD and the heatsink).

Sensor Base Standoff De-lamination

- Bonding the torlon to the gold plated heatsink without delamination after exposure to thermal cycling, random vibration and shock loads has proved to be "challenging" (It is hard to glue something to gold and have it hold up under our conditions)
- A design modification has been implemented that will add a mechanically secured, epoxy filled collar to the posted after the posts are initially bonded in place.
- Since these collars are not in the thermal Path, they will have negligible effect on system thermal performance.

Sensor Base Qual. Test Results

- In 1st sensor base qualification tests, torlon simply bonded to Au. Only normal part cleaning, no special surface treatments:
  - Result: Did not survive thermal cycling
- In 2nd sensor base qualification test, Au surface abraded before bonding:
  - Result: Survived thermal cycle & random vibration, but not shock.

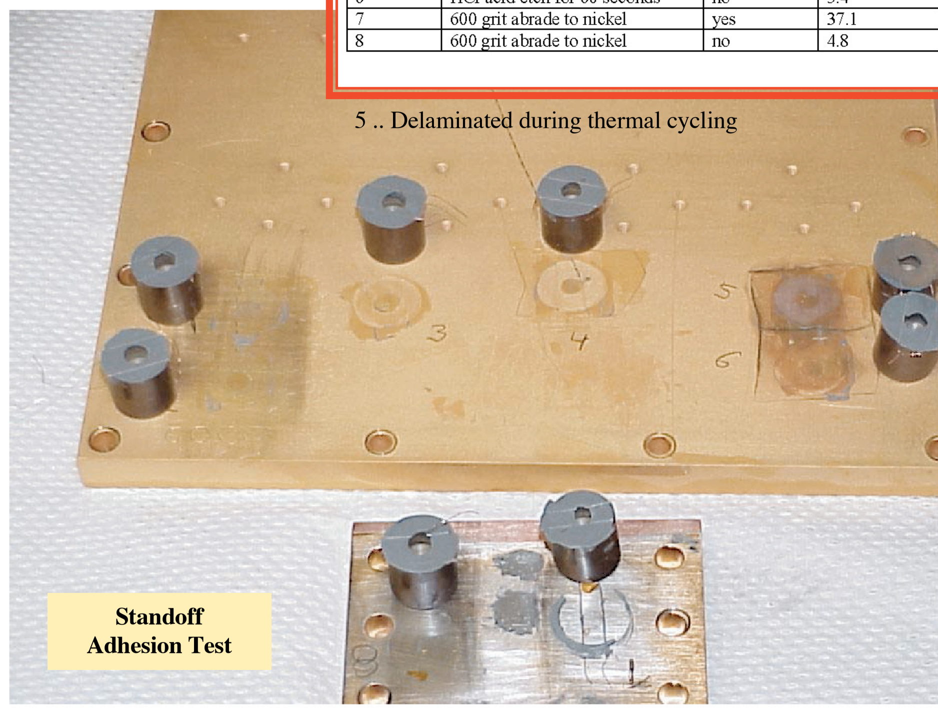
Torlon Standoff Adhesion Tests

- Decided to stop and do a series of adhesion tests before 3rd attempt to qualify sensor base.
    - Surface treatments followed by thermal cycle and static load testing
- Next Sensor Base Qualification test will include surface treatment and collars.
    – Hopefully final test! Then on to flight assembly

Test Sample Description and Results

Sample Number	Roughen Surface	Prime with Silane	Peak Load
1	600 grit abrade	yes	13.7
2	600 grit abrade	no	33.7
3	None	no	4.7
4	Nitric acid etch for 2 minutes	yes	>90.8, 44.2
5	HCl acid etch for 60 seconds	yes	0
6	HCl acid etch for 60 seconds	no	5.4
7	600 grit abrade to nickel	yes	37.1
8	600 grit abrade to nickel	no	4.8

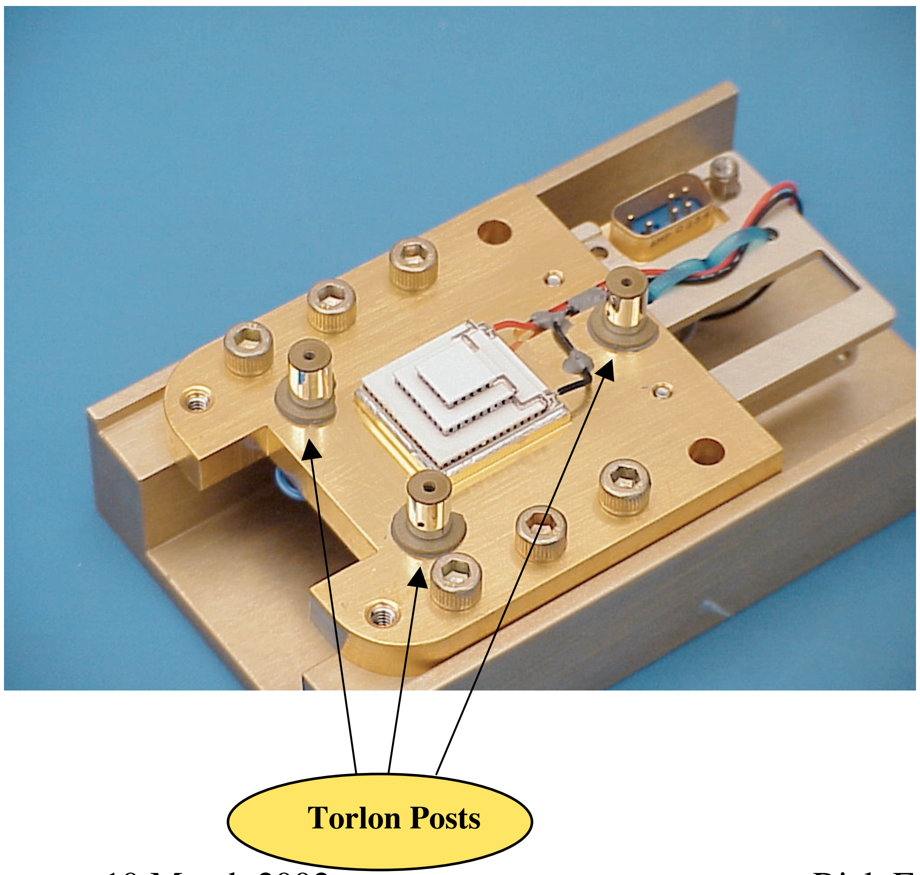
5 .. Delaminated during thermal cycling



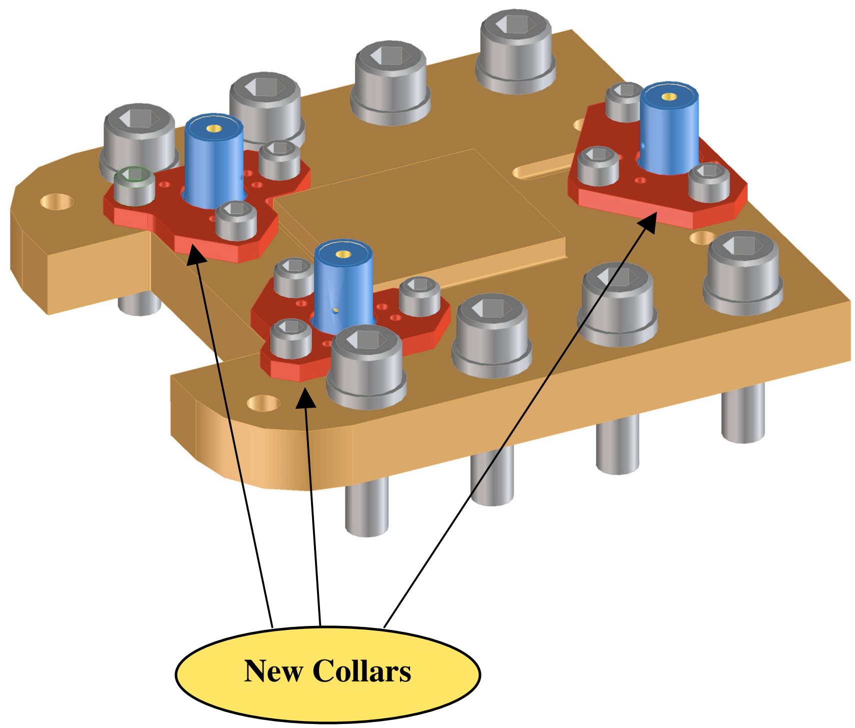
file://C:\Documents%20and%20Settings\RickFoster\Local%20Settings\Temporary%20Internet%20Files\OLK80\MVC-083X.JPG 3/5/2003

Addition of Torlon Standoff “Collars”

Revision 1 … Torlon Posts epoxied to Gold Plated Copper Heatsink



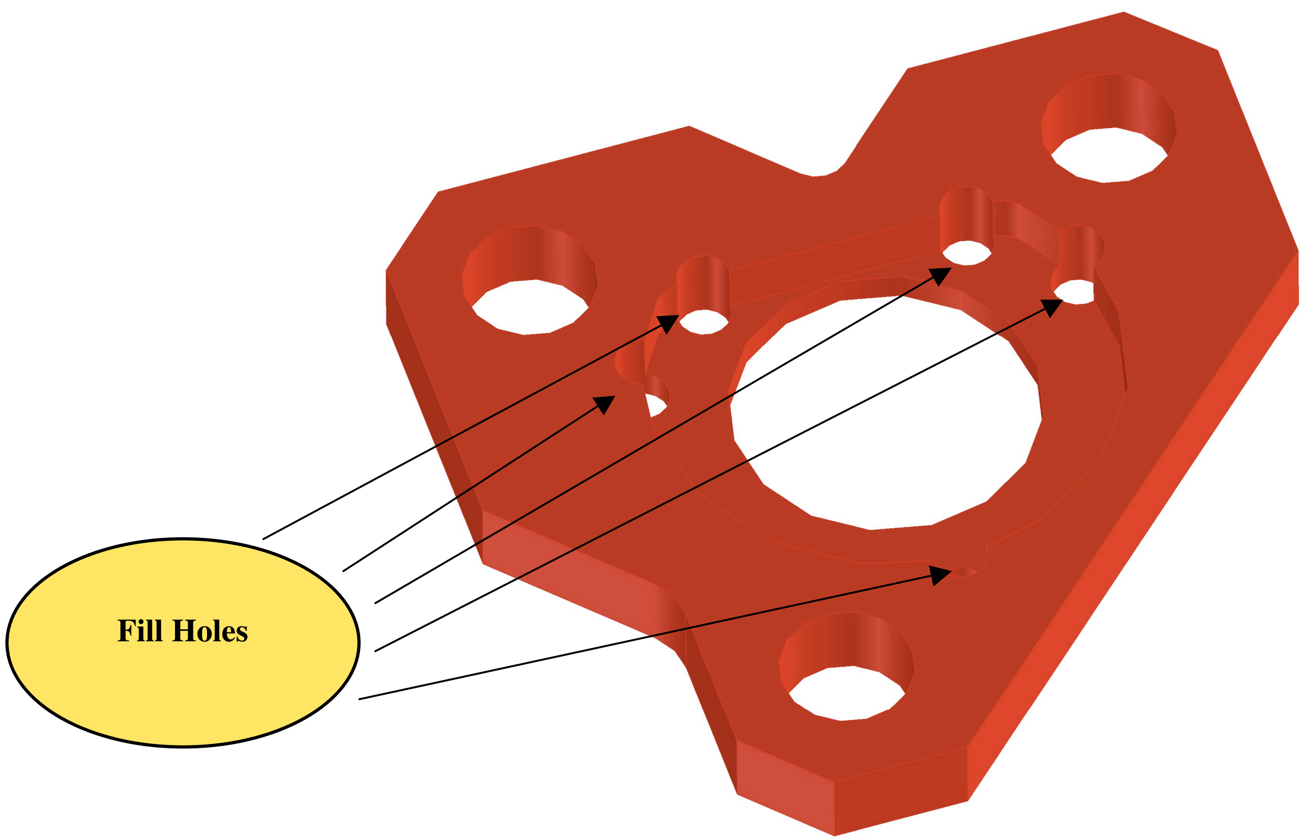
Revision 2 … Torlon Posts epoxied to Gold Plated Copper Heatsink with Au plated copper “Collar” fastened to heatsink and gap filled with epoxy



10 March 2002

Rick Foster

Collar Bottom View with epoxy fill holes



10 March 2002

Rick Foster

Analog & Thermal Control Electronics

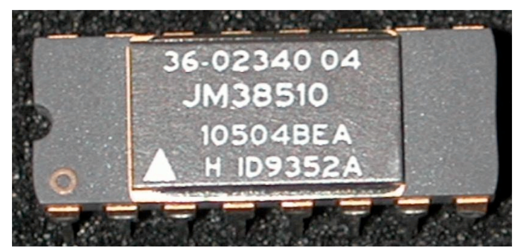
- Electronic Design is complete and project well into fabrication phase.
- No component part procurement issues
- Have had some quality problems with printed circuit board vendors.
  - One vendor closed. Fabrication of certain boards transferred to another vendor
  - Multiple coupon analysis failures from a traditionally reliable vendor have required several rebuilds of PCB by vendor
- Reviewing several ICs for additional spot shielding, with Tantalum, to improve radiation tolerance.

(NB: Ask Wada-san, Astro-F re DAC8800)

- Housings fabricated, painted and inhouse awaiting PCB completion.

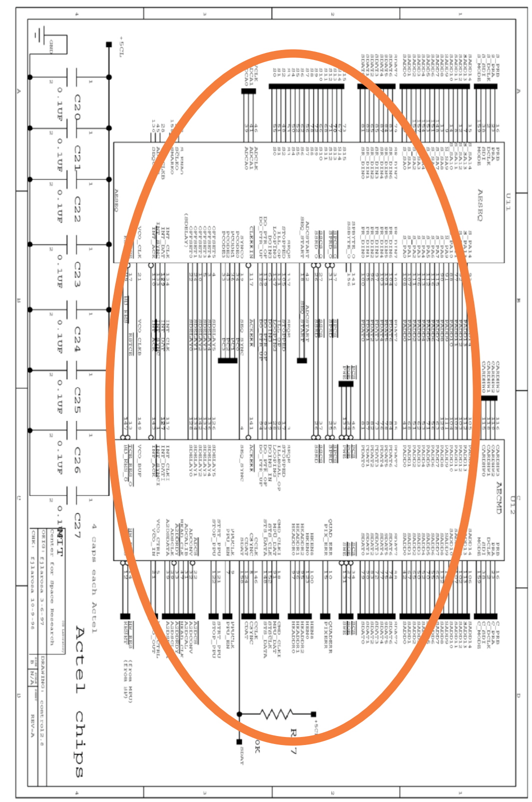
	Design	Layout	Artwork	PCB Fabrication	Assembly	Test	Conformal	System Test	
Backplane	C	C	C						Boards coupon inspection in process
Controller	C	C	C	C					
Analog Driver	C	C	C						Remake, 1st lot failed coupon
Video Processor	C	C	C	C	C				1st article test complete.
Thermal Control	C	C	C						Board coupon inspection in process

C=completed

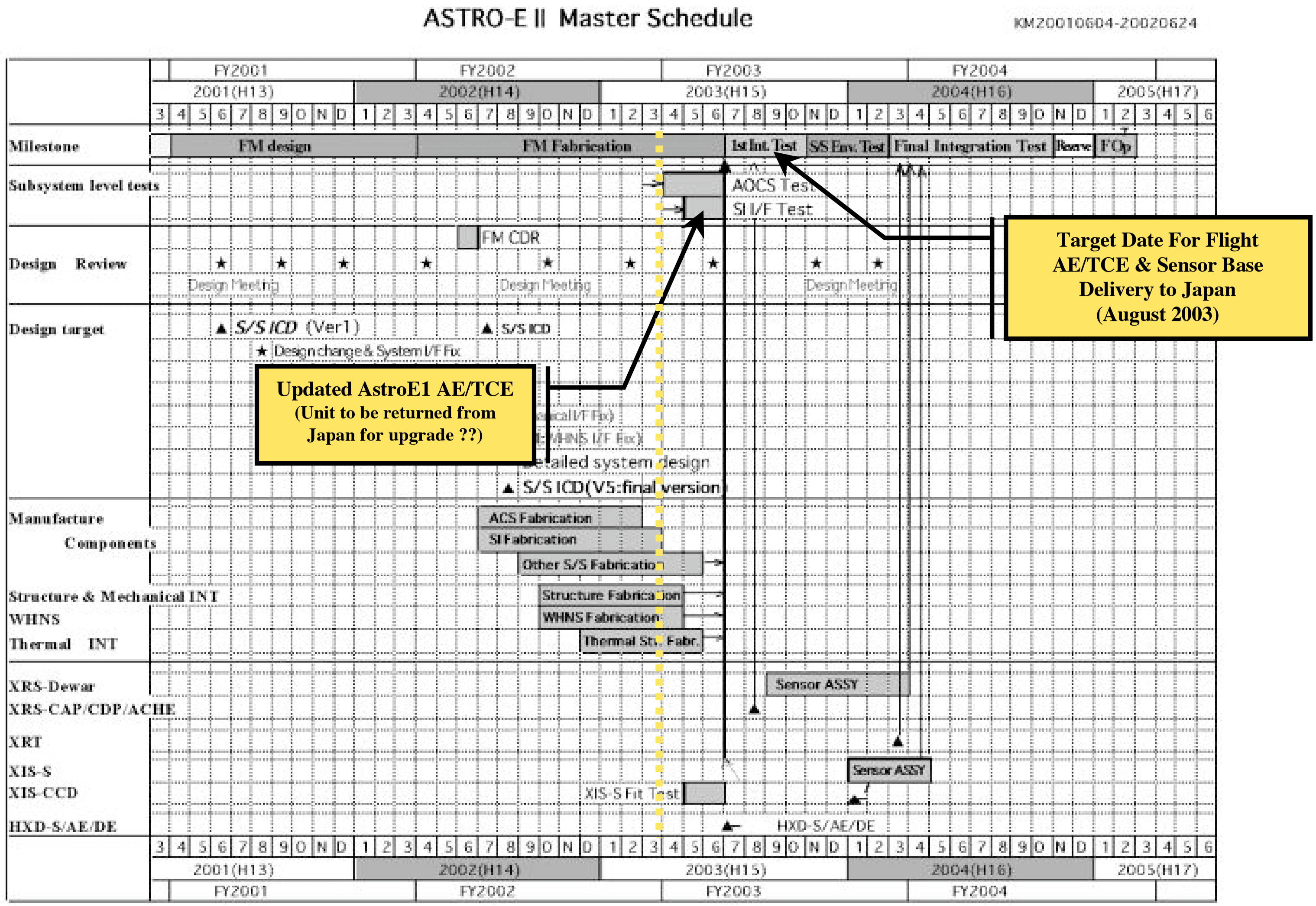


Actel FPGA

- Identified "Bugs" are in 1 of the 3 Actel1280 devices on the controller board AECMD
- AECMD is tightly integrated with other Actels and has a high gate utilization.
- It is risky to re-route the chip without comprehensive retesting: Need to test everything, not just the circuits redesigned to address bugs.
- Workaround identified for HK Read Bug
- Write-Write bug does not affect any current instrument modes.
- Decision made to use the original Astro-E XIS Actel FPGA designs.
- Actels programmed and controller boards currently being assembled.



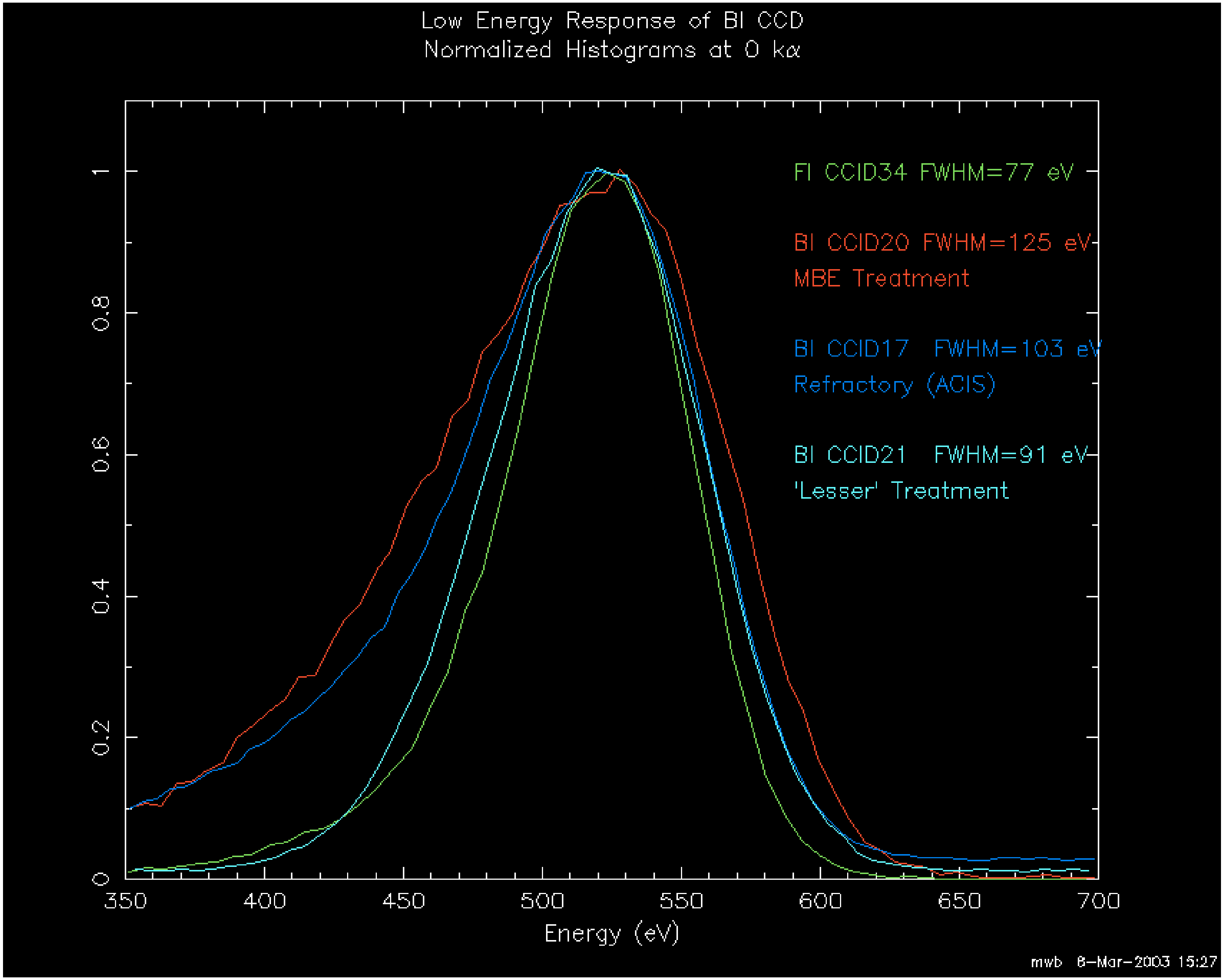
ISAS Project Master Schedule



Schedule

- Guardedly optimistic about being able to deliver the Flight Analog and Thermal Control Electronics (AE/TCE) one month early (August 2003)
  - Design and parts procurement went well.
  - Nagging quality/delivery problems with printed circuit board vendors.
- Still reviewing ability to do an early delivery of sensor bases
  - We have slowed down to investigate the standoff adhesion and detector edge glow problems.
    - Heatsink qualification should be completed end March03.
    - 1st flight sensor base assembly should begin mid April03.
- Need to finalize the details of the Japanese engineering unit AE/TCE upgrade to support integration tests activities in Japan early this summer.
  - Plan is to bring the unit to MIT, where a new Driver Board will be put in and the backplane modified.

Recent Developments in Back-illumination


Low Energy Response of BI CCD
Normalized Histograms at O kα
FI CCID34 FWHM=77 eV
BI CCID20 FWHM=125 eV
MBE Treatment
BI CCID17 FWHM=103 eV
Refractory (ACIS)
BI CCID21 FWHM=91 eV
'Lesser' Treatment
0
0.2
0.4
0.6
0.8
1
350
400
450
500
550
600
650
700
Energy (eV)
mwb 8-Mar-2003 15:27

Chemisorption for Back-illumination

In process developed by M. Lesser of U. Arizona:

- Wafer is thinned
- Back surface is cleaned & oxidized
- Thin layer of Ag (~1 nm) adsorbed on back surface
- HfO_2 coating (5 - 50 nm) deposited over Ag
- Wafer is diced and devices packaged

Experience with Lesser Coating Process

To date two LL CCD types (ccid20 & 21) have been treated with this process:

- Thinning & packaging steps done & LL
- Other steps done at Arizona

Lesser has "coated" BI devices for 3 NASA missions, though none of these has flown yet:

- HST ACS (GSFC: backup devices)
- KEPLER (GSFC)
- Lightning-Mapper (MSFC)

Process time (for coating) is about 1 week

Yield for coating claimed to be "very high" (> 80%)

BI CCDs for XIS?

- MIT will deliver 4 XIS sensor bases, plus spare, with FI CCDs, per agreed schedule.
- We have sufficient parts to build 2 additional sensor bases.
- We are investigating schedule on which BI CCDs for XIS could be available.
- Would a swap of two sensor bases (BI for FI) after September be feasible?