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To: ASTRO-E Team
Subject: Charge injection with an input register.
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1 Injection structure

In order to inject the same amount of charge into every column of the CCD, Lincoln Lab suggested to introduce a serial register at the top of the imaging array. Input diode injects charge into the serial register and when the entire register is filled, the charge is transferred into the parallel array. In this configuration the amount of charge injected into every column is defined by the same input structure and column-to-column variation is reduced to the input structure noise. The top view of the proposed structure is shown in Fig. 1 (made by Barry Burke).

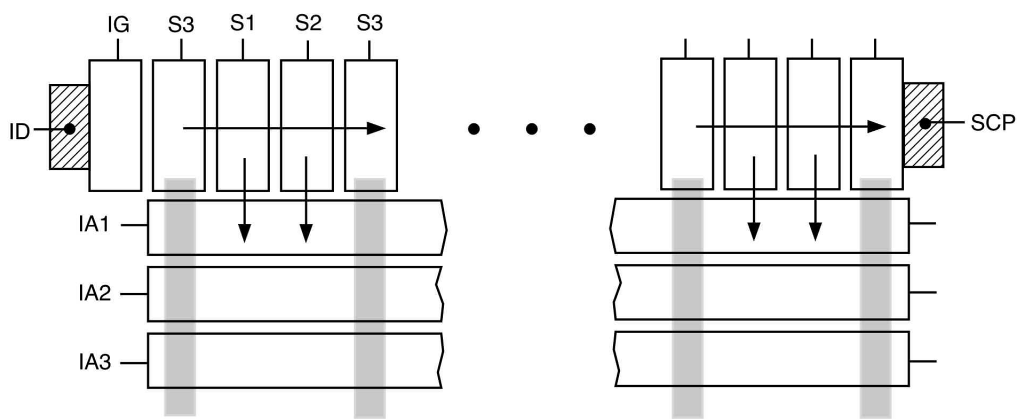

Figure 1: Top view of the input register (Barry Burke).

The details of the input structure operation are shown on Figure 2. The structure consists of an n^+ drain (Input Diode, or ID), which is a source of electrons and an Input Gate (IG) controlling the injection process. The first clocking gate S3 of the serial register is used as the second control gate of the input structure.

Injection starts when the diode potential V_D is set below the minimum of the channel potential under the input gate and electrons fill potential wells under both input gate and S3 ("fill" phase on Fig. 2). Then the ID potential is set to a higher (more positive) level (deeper potential well for electrons) and in this "spill" phase the charge above the input gate depletion potential (second

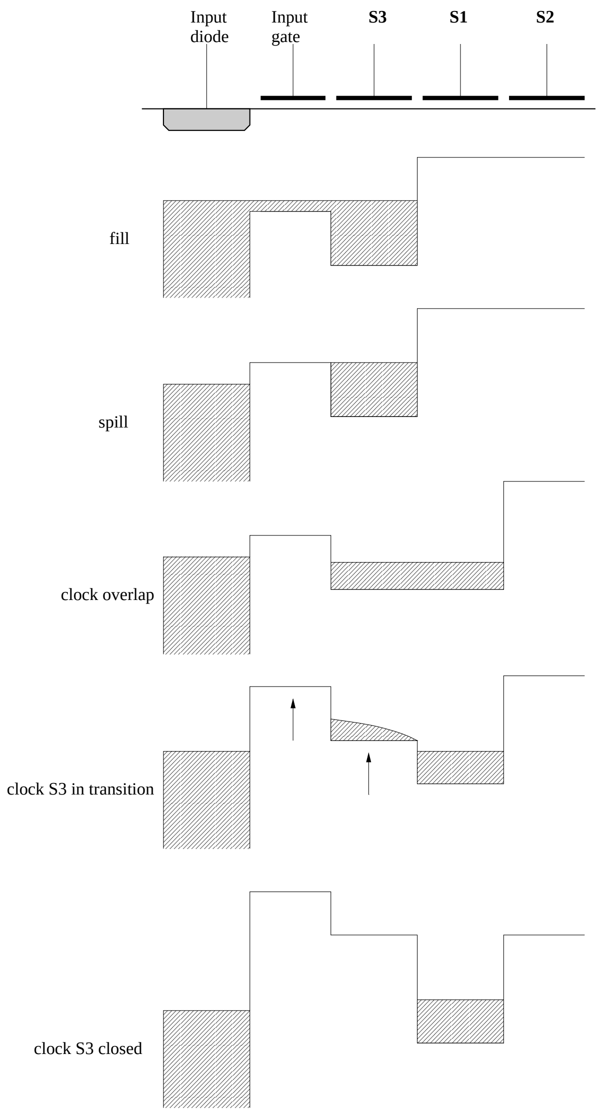

Figure 2: Injection of charge into the serial register.

lower plot in Fig. 2) spills back into the diode. The difference between channel potentials under the gates IG and S3 determines the amount of charge injected into the register and because of that it has to be controlled by a DAC. The next phase of the input cycle is an overlap (in time) between the clocks S3 and S1, when S1 goes open (high). At this time earlier injected charge spills under both of these gates. Then the clock S3 starts to close (go low) and the signal charge flows under S1. If the IG stays at the same potential it is very likely that some of the signal charge from under S3 will flow back into the ID as S3 moves to the low state. To prevent this we suggest to move IG synchronously with S3, maintaining the same voltage difference between the two gates. In other words, voltage on the IG should be connected to the S3 through a follower with a constant offset. The offset must ensure that potential under IG is less positive than under S3.

The input register does not have the trough doping. This means that the channel potential under the gates is slightly lower than under the same gates in the output register. It also means that when the radiation damage is accumulated, transfer efficiency for small charge packets will be very poor. To maintain the same amplitude of signal charge over the entire length of the input register it has to be overclocked.

Since the amount of charge that we need to controllably inject is extremely small (on the order of 100 electrons), the most difficult task is to set the limits for the offset voltage between IG and S3. According to Barry the sensitivity of the input structure is on the order of 100 $electrons/mV$, so the step of DAC must be of the same order, something like $1mV/digit$. At the same time there are at least two additional mechanisms which can introduce significant internal offsetts to this voltage. One of them is depletion potential difference under different levels of polysilicon. Depletion potential for current techology is the highest under poly 1, the lowest under poly 3, the difference can be as big as 0.5 Volts (Barry Burke) and is caused by slightly different thicknesses of gate dielectric (SiO_2 under poly 2 and 3 is slightly thinner since it subjected to additional etching when the poly 1 is removed). IG and S3 necessarily have to be made of different polysilicon layers and the potential difference has to be compensated in the off-chip circuitry.

Another source of offset is caused by the "evaporation" of electrons from the potential well filled with charge. This phenomenon takes place when the spill phase is over and electrons under the gate S3 are waiting to be transferred away. Electrons with energy high enough to go over the potential barrier formed by the IG can leak into the ID, thus making a potential well under the S3 effectively more shallow. This process is described in a paper [1]. The authors report for their structure and timing (which are different from ours) a 0.5 V difference between the well and the barrier. This offset must also be compensated by external circuitry.

The difference in depletion potential under different levels can be used to alleviate the charge transfer and reduce the probability of electrons to "evaporate" during the clock overlap if the gate S3 is made of polysilicon 3. Then the potential well under S1 is deeper and most of the charge will flow there immediately after opening the gate S1. This may require adding one or two extra gates to the register.

2 Changes in the electronics.

The proposed scheme requires clocking the ID. Input gate also is clocked, but it does not need a separate sequencer channel: it can follow the S3 clock. Two DAC controlled levels are needed: one for the low level of the ID (it determines the onset of charge injection). The second one (offset voltage of the IG relative to the S3) defines the depth of the potential well for the signal charge and, hence, its magnitude. As it follows from the discussion above this offset needs a fine adjustment with a DAC to control the amount of injected charge. There also must be a possibility to crudely adjust this offset individually during the device calibration, probably with resistors. The range of this coarse adjustment is about $\pm 1 - 2$ Volts.

High level of the ID can be kept at the same voltage at all times. The only requirement is that it must be higher than the depletion voltage in the channel under IG when it is at high level. This requirement would be satisfied at some sufficiently positive voltage, say +15 Volts. The high level of ID could be set equal to the scupper bias.

The gates of the input serial register can be connected with the corresponding gates of the output serial register since injection can be prevented during the output register readout by holding the ID high.

Here is a table summarizing the voltage requirements described above.

Signal	Level	Adjustable in flight?	Range, V	Accuracy, V	Remarks
ID	high	no	+12	0.1	Const voltage
ID	low	yes	$0 - +12$	0.1	Controlled by separate DAC
IG	coarse	no	$S3_{high} \pm 2$	0.1	Tuned via resistors on driver board
IG	fine	yes	$S3_{high} - S3_{high}$-0.25	0.001	Controlled by separate DAC

References

[1] S. Kawai, N. Mutoh, N. Teranishi, "Thermoionic-Emission-Based Barrier Height Analysis for Precise Estimation of Charge Handling Capacity in CCD Registers", IEEE Trans. on Electron Devices, vol 44, No. 10, 1997, pp. 1588-1592