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To: ASTRO-E Team
Subject: Charge injection structure for the redesigned ccid17.
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Our ACIS experience showed that a charge injecting structure at the top of imaging array is a highly desirable feature that may help to alleviate the consequences of the radiation damage in a CCD. In this memo I review different possibilities of how such a feature can be implemented in the new reincarnaiton of the CCID-17.

1 Charge injection structure

The most common "fill-and-spill" scheme of charge injection process is shown on the left on Fig. 1. The structure includes an n^+ drain which is a source of electrons and two gates controlling the

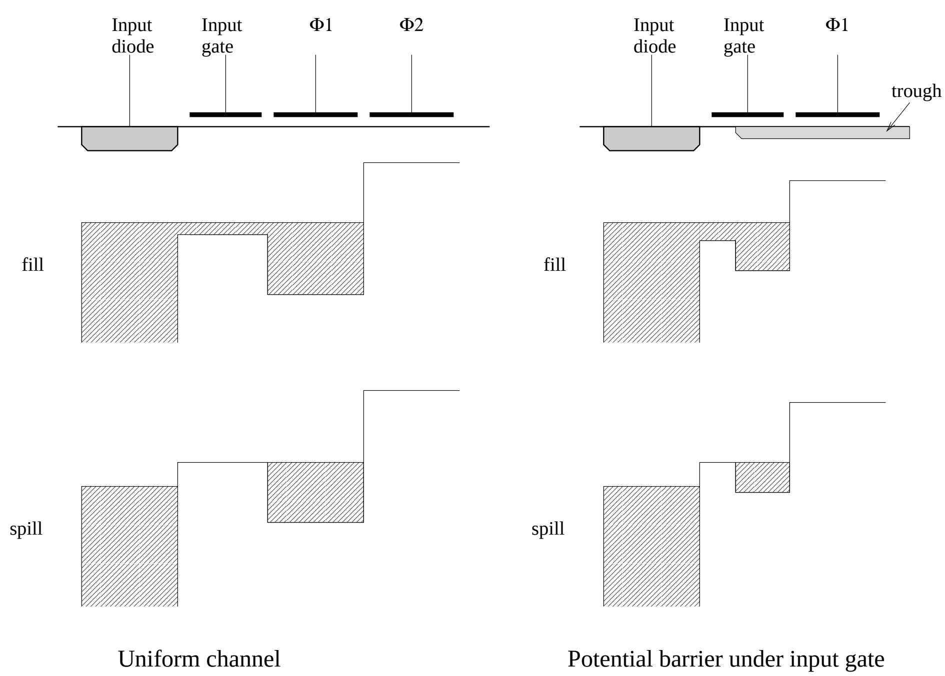

Figure 1: Injection of charge through the input diode structure.

injection process. The first clocking gate $\Phi 1$ of the imaging array can be used as the second control gate of the input structure. Injection starts when the diode potential V_D is set below the minimum of channel potential under the input gate and electons fill potential wells under both input gate and $\Phi 1$ ("fill" phase on the Fig. 1). Then the diode potential is set to a higher positive level (deeper potential well for electrons) and in this "spill" phase the charge above the input gate depletion potential (lower plot in the Figure 1) spills back into the diode. This technique requires the diode to be clocked while input gate remains at a constant potential. It is possible to do it in a different way - to keep the diode at a constant potential and clock the gate. In this case the "fill" phase is the same, but instead of increasing the diode voltage during the "spill" time, the gate potential is moved to more negative level (up in the diagram, which physically corresponds to the less positive level) in order to cut off the diode from the gate $\Phi 1$.

Devices made by Lincoln Lab normally have so-called trough that confines signal charge to a narrow region around the center line of the pixel. This is achieved by doping the buried channel in the central part of the pixel to a slightly higher degree than the rest of the buried channel. This additional level of doping presents an opportunity to introduce a potential barrier in the middle of the input gate (see Fig. 1, right). If the trough doping stops in the middle of the input gate then "fill-and-spill" cycle would always inject fixed amount of charge into such input structure. The length of the potential well under the input gate should be the same as the length of the smallest gate in the array (5 microns, the length of the gate in the frame store section), in this case the injected charge will fill the entire volume of the trough and would not spill into the rest of the buried channel. An advantage of this technique is that no calibration of the input structure is required, it always injects the same amount of charge to just fill the traps inside the volume of the trough. It also eases requirements to the voltages applied to the input gate and the diode (they will be discussed below). The disadvantage of this approach is that it becomes a tricky task (not impossible, though) to inject any smaller amount of charge. Currently we do not see any reason, though, to inject small charge packets. Because of that we suggest the structure with potential barrier to be used and the following considerations will be made under this assumption.

2 Voltage requirements.

Injection of charge always needs to be done during parallel transfer when voltage levels at the parallel gates are switched between $+5$ and -5 Volts. Entire "fill-and-spill" cycle must be performed during the time when the first gate of the image section $\Phi 1$ stays closed (kept at low level of -5 V), otherwise much larger amount of charge could be injected under the $\Phi 1$ unless the diode is biased to very high positive voltage.

Only one of the two electrodes (Input diode or Input gate) needs to be clocked in order to inject charge. For a moment, though we allow both of them have two levels – high and low – and use the corresponding indices (h or l) as superscripts in the voltage and potential notation below. Another notation convention used below is that letter V refers to voltages applied directly to the electrodes and letter φ is used for the corresponding potentials in the channel.

It is imprtant to keep in mind that fill phase corresponds to low voltage on the diode and high voltage on the gate; spill phase corresponds to high level on the diode and low level on the gate. Later we can decide which of the two electrodes will be kept at a constant voltage, declaring that the high and the low levels are the same. That would not change the relations formulated below.

For the fill phase two conditions must hold. Input diode should never be able to inject charge under the closed gate $\Phi 1$ because this would fill with electrons an entire CCD array. This means that low voltage level V_D^l on the input diode has to be greater than channel potential $\varphi_{\Phi 1}^l$ under the gate $\Phi1$. On the other hand, at this level on the diode injection under the input gate has to take place, which means that the channel potential φ^h_{IG-b} under the barrier portion of the gate that has no trough must be more positive then the diode voltage: $V^l_D < \varphi^h_{IG-b}$.

In the spill phase we can write down three more conditions: the diode voltage V^h_D must be more positive than the potential under the barrier (no trough) portion of the gate in order to allow the excess of electrons to flow back into the diode. This means: $V^h_D > \varphi^l_{IG-b}$. This same low level on the gate must allow electrons from the well portion of the input gate (with trough) later to flow under clocking gate $\Phi1$ when it opens. When all the electrons are transferred under the gate $\Phi1$ the channel potential there will increase by amount $\Delta\varphi_M$. The signal charge under the Input gate is will be slightly less than the charge necessary to fill the trough under $\Phi1$, which means that $\Delta\varphi_M$ is a little less than the difference between the well and the barrier potentials $\varphi_{IG-w} - \varphi_{IG-b}$. We will assume this difference to be 2 Volts. This requirement can be written as $\varphi^l_{IG-w} < \varphi^h_{\Phi1} - \Delta\varphi_M$.

Finally, the potential under the barrier portion of the Input gate while it is in low state must be more positive than the potential under the closed first gate of the array $\Phi1$, otherwise the charge will spill into the imaging array before the opening of the gate $\Phi1$: $\varphi^l_{IG_b} > \varphi^l_{\Phi1}$.

Now, let's rewrite the above formulae depending on which of the two electrodes is clocked.

a) Input diode at constant voltage ($V^l_D = V^h_D = V_D$).

$V_D > \varphi^l_{\Phi1}$	prevents injection into array
$V_D < \varphi^h_{IG-b}$	garantees filling of the IG well
$V_D > \varphi^l_{IG-b}$	insulates diode from the IG well and array
$\varphi^l_{IG-w} < \varphi^h_{\Phi1} - \Delta\varphi_M$	garantees charge flow from IG into array
$\varphi^l_{IG_b} > \varphi^l_{\Phi1}$	prevents leaking charge from IG inot array

b) Input gate at constant voltage ($\varphi^l_{IG} = \varphi^h_{IG}$).

$V^l_D > \varphi^l_{\Phi1}$	prevents injection into array
$V^l_D < \varphi_{IG-b}$	garantees filling of the IG well
$V^h_D > \varphi_{IG-b}$	insulates diode from the IG well and array
$\varphi_{IG-w} < \varphi^h_{\Phi1} - \Delta\varphi_M$	garantees charge flow from IG into array

The dependence of the maximum channel potential on the gate voltage was measured for the output gate of the ccid10 during the preliminary stages of ACIS development. The results were described in my ACIS memos 41 and 44. It was found that when the surface is not inverted the dependence can be approximated by the function

$$\varphi_{channel} = 0.85V_{gate} + 7.14$$

in the trough region. While this dependence would differ slightly in the narrow channel region of the imaging section, it is a reasonable first order approximation. For the no-trough region for the purpose of crude estimates we will assume that the channel potential is shifted down by 2 Volts from the trough region.

Having written down the voltage limitations we can try to choose levels that will satisfy the above conditions.

In case a) the set of voltages:
$V_D = +7$ V,
$V_{IG}^l = -3$ V,
$V_{IG}^h = +4$ V
looks quite reasonable.

In case b)
$V_{IG} = 0$
$V_D^l = +4$ V
$V_D^h = +10$ V
levels would satisfy all the conditions.

I believe it is preferrable to keep the input diode at constant voltage, clocking the Input gate only.

Slight adjustments of the voltage levels indicated above will be necessary during the initial device testing stage, but the changes would not be very significant.

3 Proposed changes in electronics.

As discussed above, there are many different ways to implement the charge injection. Assuming that some changes in the electronics are acceptable, the following scheme is a suggestion how to use the available resources. We will assume that the Input gate has a potential barrier (Fig. 1, right); also the scheme with the constant diode voltage is adopted for further discussion.

There are 2 DAC regulated levels currently available in the ASTRO-E electronics. One of these levels should to be assigned to the input diode voltage level V_D. The diode voltage would be kept constant at all times. DAC regulator provides voltage in the range from 0 to +12 Volts, which is completely adequate for the input diode.

Second DAC regulated level should control the low level of the Input gate because this level may depend on the variable technological parameters like doping level and may require adjustment. The suggested voltage range for this level is from -7 to 0 Volts (it could be -12 to 0, if that is easier from the design point of view). High level of the Input gate voltage can be fixed at some reasonable positive potential, say +7 Volts. The only requirement to this voltage is that channel potential in the barrier region at this voltage must be higher than the diode voltage, and that would be easily achieved.

In principle, the levels for the Input diode are about the same as the levels currently used for the serial clock (-3 +7 Volts). While it does not seem to solve any of the design problems, it is possible to use serial clock DACs to control the Input gate voltage levels.

Finally, one of available sequencer channels must be used to clock the Input gate.