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To:	MIT XIS Team
From:	Mark Bautz
Subject:	Summary of Charge Injection Review Meeting

Here are conclusions and action items from our meeting today concerning charge injection.

Conclusions

- We agreed that the input gate driver circuit (see Figure 1) was acceptable with the following stipulations:
  - ⋆ *Offset resistor locations:* Provision will be made to mount the coarse offset adjustment resistors (R27 and R29) on new, a sensor-specific external connnector on the AE/TCE box. We'll have one such connector for "side" of the AE. This will allow us to adapt the coarse offset adjustment to each sensor base by simply attaching a suitable external connector. Ed will work out details.
  - ⋆ *Coarse adjustment range:* As currently drawn, the circuit provides a coarse offset adjustment range of about $\pm 1V$. John believes changes in passive component values can increase this to ± 2 V without affecting the resolution of the fine adjustment. John will investigate and propose changes to Ed to obtain a ± 2 V range.
- *The input diode bias* will be adjusted only via a DAC (not by sequencer driven clock signal.) To defeat charge injection we will set the ID potential high, via a dedicated DAC, (to +12 V or higher). To enable charge injection we will set the ID to a fixed operating point (approximately 6 V or so). With the ID at this operating point, we will control which lines contain injected charge by stopping and starting the serial register.
- *Input register transfer direction:* The input register clocks will be taken from the serial register clocks. The connections will be made so that, when the output register is clocking in the normal mode for taking science data, the input register will be clocking charge backwards (i.e. toward the input diode.) To inject charge, therefore, we will run the output register backwards. *This is a change from our agreement at the meeting.* The intent of this arrangement is to reduce the risk that charge would be injected inadvertently in the event that a DAC failure makes it impossible for us to to run the ID to a sufficiently high bias. To summarize, we want the input register to be moving charge in the same direction as output registers serving output nodes A and C.
- *Two additional telemetry channels* will be instrumented for the charge injection circuitry, as follows. (This will leave one remaining unused channel.)

- ⋆ Input diode bias.
- ⋆ Input gate current (details TBD by John Doty).

- *The input gate driver test sequence* is to be as follows:
  - ⋆ Breadboard test complete by MIT XIS PDR. Will verify IG-to-S3 offset command capability, with ~ 300 mV precision.
  - ⋆ Laboratory "daughterboard" for use with calibration GSE in building 37 by early July.

Action Items:

- John Doty to suggest to Ed Boughan IG driver changes to allow $\pm 2V$ coarse adjustment.
- John Doty to define telmetry requirements and approach for input gate current.

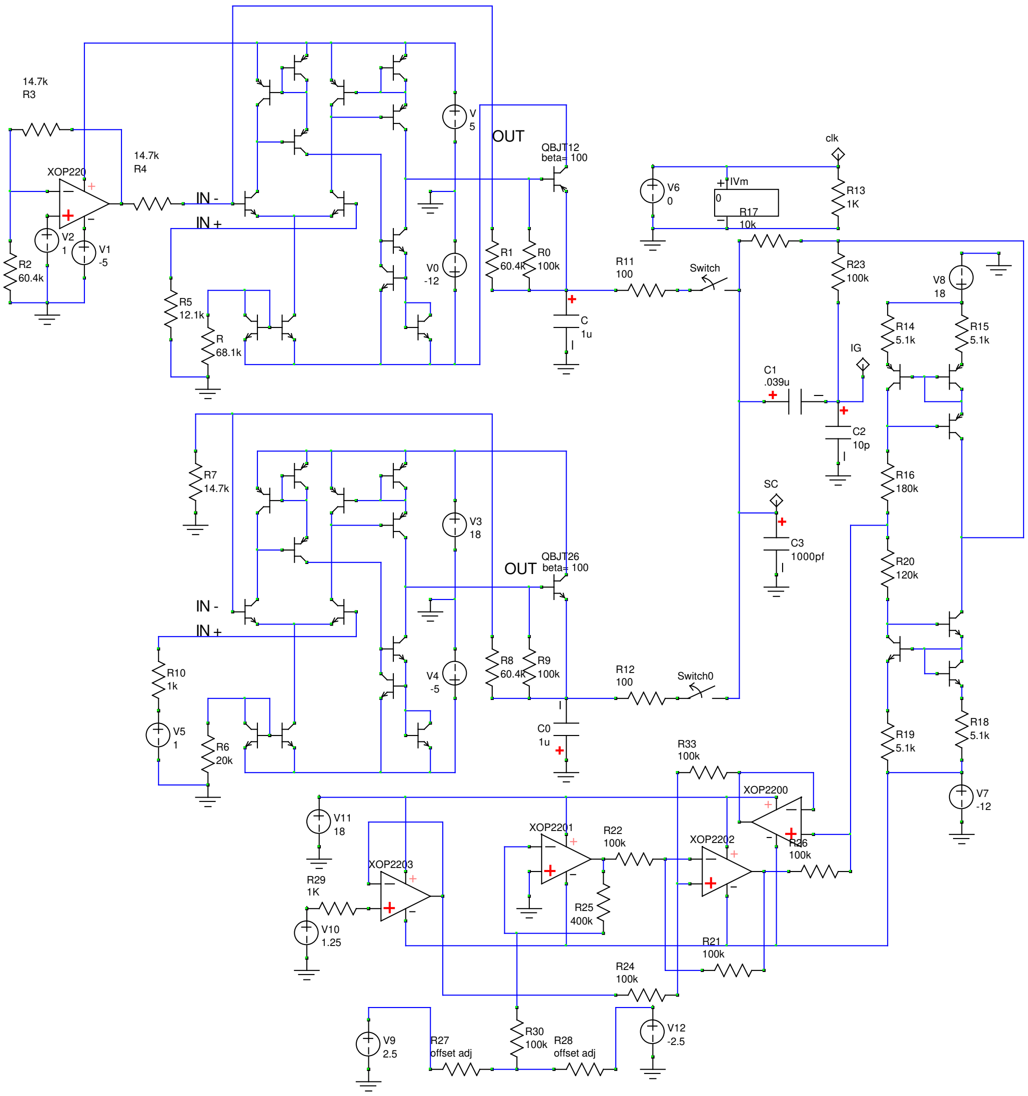

Figure 1: Input gate driver circuit from Ed Boughan's email of 24 May; desirable changes to this circuit are discussed in the text