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To: XIS Team
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Subject: Charge Injection Users's Overview

Summary

The XIS2 CCD (Lincoln Laboratory model CCID41) contains a charge injection register for the purpose of ameliorating and calibrating the effects of radiation damage. Several earlier memos (PS4 of 5/29/02; PS3 of 1/18/02, both available at `http://space.mit.edu/ACIS/ixis.html`) described initial ideas for implementing the charge injection electronics drive circuitry in the XIS2 analog electronics (AE). The final design differs in some important respects from these early ideas. The purpose of this memo is to summarize the final implementation of the electronics from the point of view of the XIS user. Discussions of some of the physical principles involved, and of the details of the electronic design, are contained in the references cited above.

Charge Injection Signals

The charge injection structure on the CCID41 is shown schematically in Figure 1. This structure comprises an input diode (ID) and input gate (IG) near the upper left edge of the device as well as a 3 phase input serial register (IS1-IS3) extending across the top. Also, an extra parallel phase 3 (IA3) is inserted between IS and the top row of the image array (IA).

Input Diode: This diode is the source of injected charge. Its voltage can be set to a high or low level depending upon the status of the sequencer bit 7 (b7) and the driver control register injection disable bit (D_CR_CHAN0 bit 0). If the injection disable bit is set (D_CR_CHAN0 bit 0 = 1) then ID will default to the high voltage level regardless of sequencer b7. If cleared (D_CR_CHAN0 bit 0 = 0) ID will be controlled by b7 with b7 = 0 corresponding to high voltage and b7 = 1 to low voltage. The actual values of the ID high and low voltages (18 volts and 10 volts approximately) are fixed and cannot be changed by the user. The actual functioning of the charge injection is not sensitive to these values.

Input Gate: The input gate resides between the ID and the first phase (S3) of the input register. It controls the amount of charge injected during "fill and spill". IG is tied to IS3 (on the driver board and via a coupling capacitor on the flexprint) so that the clock timing of IG and IS3 will be the same. Also, the voltage level of IG will follow that of IS3 except that a small offset voltage can be added to IG via driver dac channel 11 (D_DAC_CHAN11). The circuit is adjusted so that D_DAC_CHAN11 = 255 corresponds to the minimum injected charge desired and D_DAC_CHAN11 = 0 to the maximum. This adjustment is made by means of resistors housed in plugs on the electronics housing, and so may be changed before installation of the XIS on the spacecraft. This allows us to compensate for CCD-to-CCD variations in the CCD threshold voltage. Thus the IG drive circuit can be (and is intended to be tuned for each individual CCD.

The relation between dac level and injected charge is not linear; there is more control for small charge levels. See the discussion of performance below.

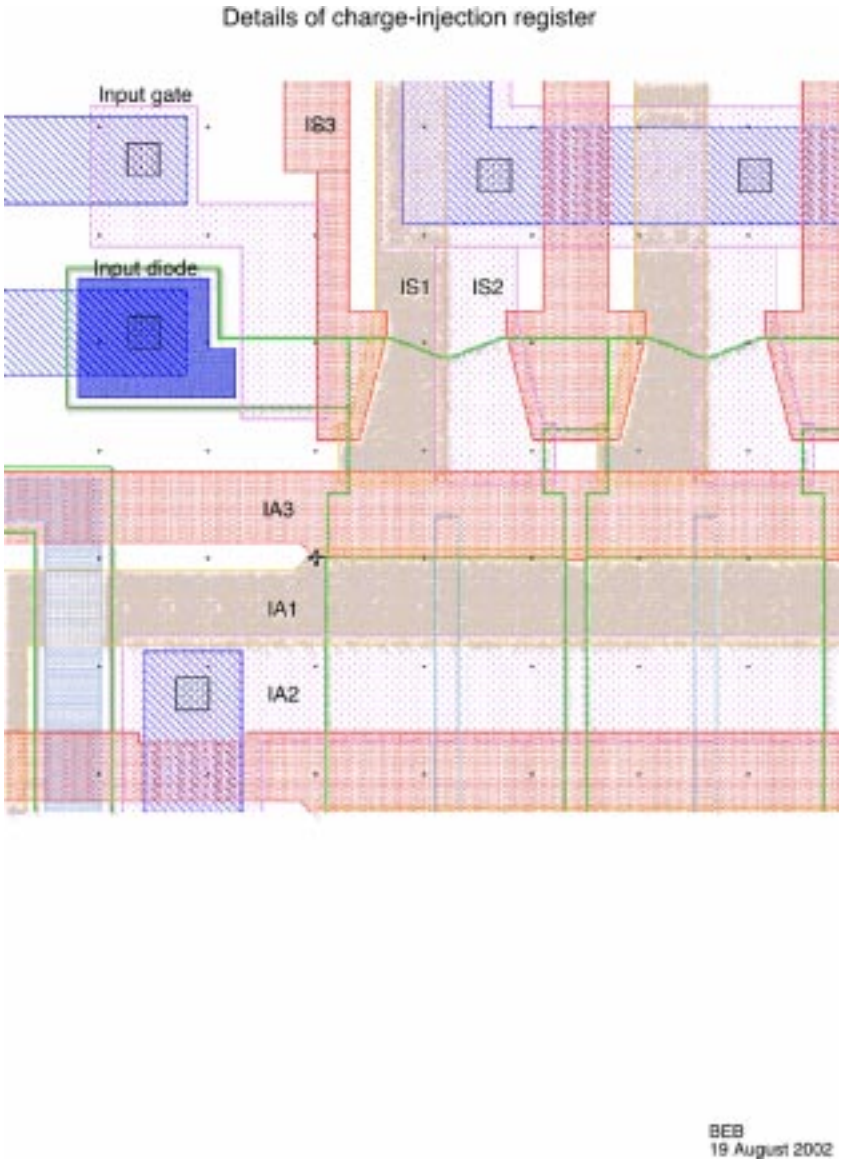

Figure 1: Schematic of charge injection structure on CCID41, courtesy of Barry Burke.

IS1-IS3: The injection serial register is analogous to the output register except it is unidirectional and not split. IS phases are connected directly to the output register so that normal readout operation of the output register results in input operation of the input register. The voltage level and timing of the input register are controlled by the output register dac and sequencer bits. There is no independent control of IS.

Sequencing

The "fill & spill" method of metered charge injection, illustrated in Figure 2, starts with ID and IS3 high, IS2 low. ID is then brought low via sequencer b7 (injection disable bit is off). The potential well under IG and IS3 will be filled with charge. IS2 keeps charge from leaking further into IS. ID is then brought high. The charge under IG and IS3 will spill back into ID. If IG is slightly lower voltage than IS3 then a small amount of charge will be held under IS3. The amount of this charge is controlled by the voltage difference between IG and IS3 via D_DAC_CHAN11. This

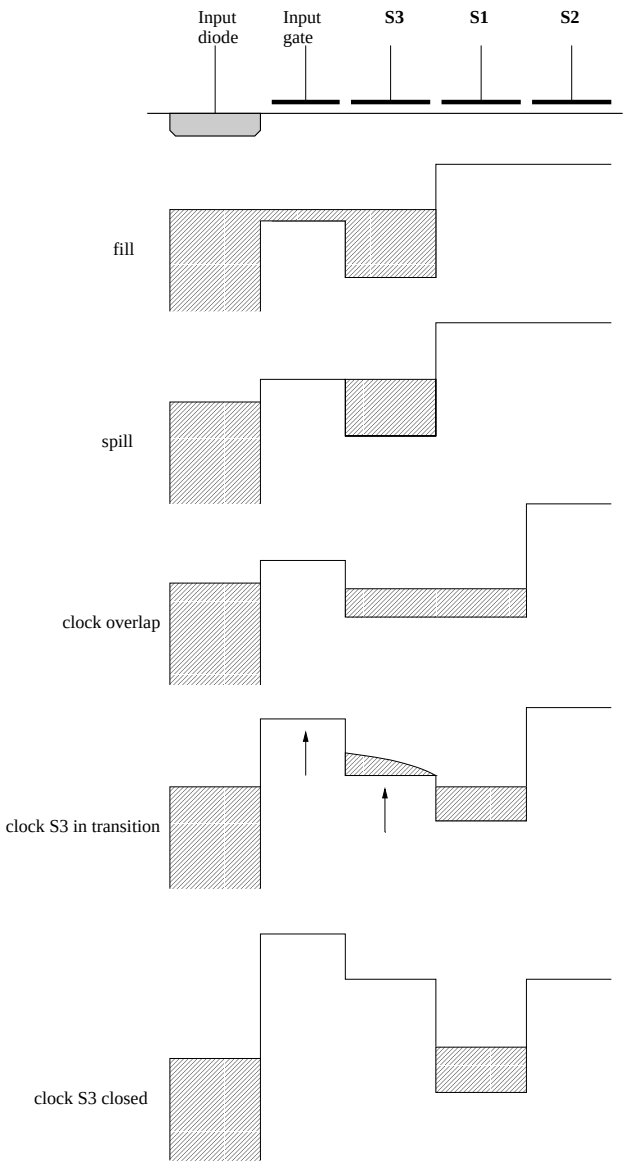

Figure 2: "Fill & spill" sequence used to inject charge into the input register.

charge can then be moved along IS in the normal fashion with additional injection as required. When a row of charge (or pattern) is created in IS these charges are blocked from the top row of IA by IA3 (normally low). IA3 is then brought high and the injected row is "lifted" by bringing all 3 phases of IS low. The injected row is then moved to parallel phase 2 of IA and parallel IA3 returned to low level. The injected charge now resides in phase 2 of the top row of IA. Bear in mind that when discussing voltages during fill-and-spill it is the voltage in the buried channel that is meant.

Performance

Figure 3 illustrates a typical injection characteristic for one flight candidate sensor, as measured with calibration (i.e., non-flight) electronics. In this case the minimum quantity of injected charge is over 100 adu (1 adu corresponds to roughly 1 electron) and further adjustment of the compensation resistors, to lower the minimum signal level, is clearly desirable. The RMS variation of the injected

charge, from a 15 samples in each of 256 columns, is shown in Figure 4. The input gate structure allows injection with a precision of 10 electrons, RMS, or better, at the lowest signal levels.

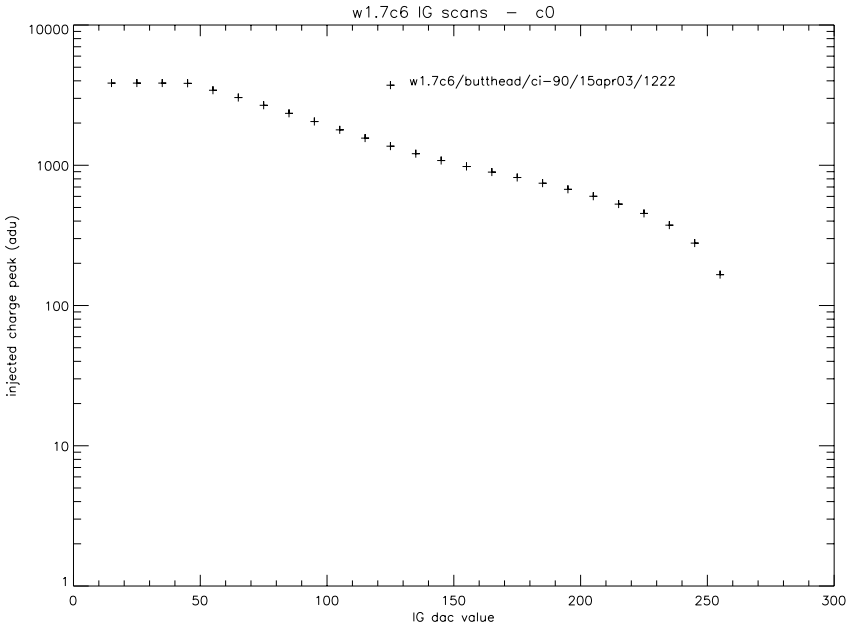

Figure 3: Mean injected charge in adu (1 adu $\approx$ 1 electron) as function of the IG DAC (D_DAC_CHAN11) setting for a flight candidate CCD. The minimum injected charge is greater than 100 electrons, but could be reduced by changing the external compensation resistors on the electronics.

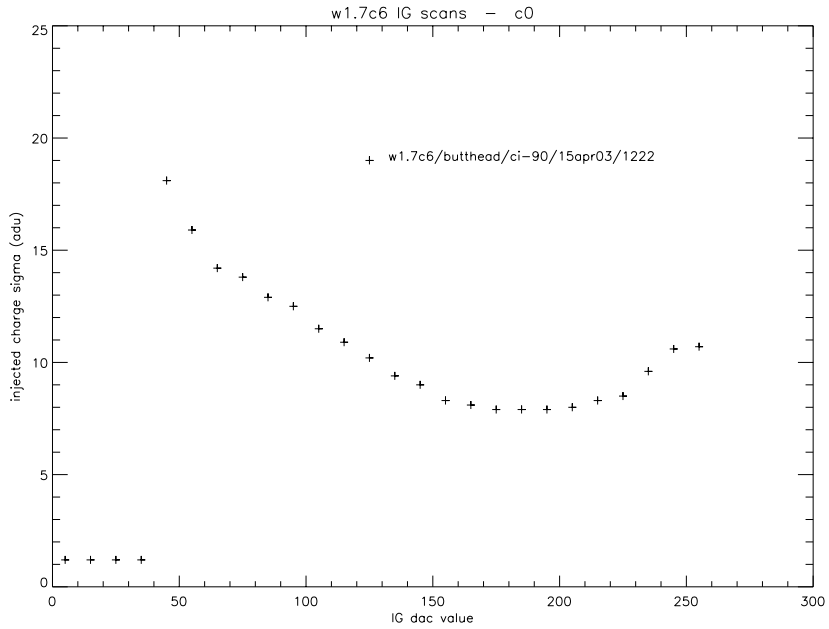

Figure 4: RMS variation of the quantity of injected charge as a function of the IG DAC (D_DAC_CHAN11) setting for a flight candidate CCD.