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To: APS Team
From: Mark Bautz
Subject: APS test system based on XIS AE?

Summary

This memo summarizes recent discussions on how the XIS analog electronics might be adapted to serve allow testing of MIT Lincoln Lab Active Pixel Sensors (APS) at CSR. The sensor in question is described in a recent memo by Vyshi Suntharalingam (24 Jan 2003; see <http://space.mit.edu/ACIS/aps.html>, hereafter this memo is referred to as VS.) The ideas outlined here are certainly preliminary, and the main purpose of this memo is to identify the requirements which must be specified before an APS test system can be designed.

Video Processing

The video output of the test sensor described by VS differs in several important respects from that of a CCD. First, the maximum bias applied to any of the transistors is 3.3V, so the DC level of the signal is a few volts at most. Second, although the device contains an on-chip video signal processor that provides signal and “reset level” in separate outputs, true correlated double sampling is not possible.¹ Third, the responsivity of the device is likely to be lower than that of typical Lincoln CCD amplifiers.

Under these circumstances, it seems that the “analog video processor” of the existing XIS electronics (as defined, for example, on “video digitizer” drawing of the XIS video board) is not well-matched to the APS.

Suggestion: One approach might be to replace the XIS “analog video processor” section with a low-noise differential amplifier. The signal and reset outputs of the detector would be applied to the inputs of this amplifier; the output of the amplifier would be suitable for connection to the “AIN” input of one of the existing A/Ds on the XIS video board. Since there are 3 other digitizers on an XIS video board, it might also be useful to be able to digitize the signal and reset waveforms separately as well, using two of the other A/Ds on the board. To do this, some provision for subtraction of an (ideally programmable) offset from these signals would be needed. Would it be possible to put such a differential amplifier on a daughter card, and use a (partially populated) XIS video card for the digitization?

¹In fact, the on-chip video processor can sample and hold the reset-levels of all 256 pixels in a selected row simultaneously, and then sample and hold signal levels of all of those pixels. One can then sequentially “read” these values for each pixel in the row, one pixel at a time, using the single pair of outputs present on the device. Since separate capacitors are used to store the signal and reset levels, respectively, of each pixel, uncorrelated “kTC” noise components are introduced in each; these noise components will not cancel when the reset level is subtracted from the signal in subsequent (off-chip) processing. The magnitude of the residual kTC noise is likely to be a few dozen electrons, RMS.

Note: We do intend in future APS sensors to include true double correlated sampling, but this must be done on-chip.

Address Lines

It is neither feasible nor desirable to use a separate XIS sequencer bit for each of the 16 address lines required by the test APS.

Suggestion: An address generator using, say, 4 sequencer bits as input (e.g. for row-reset, row-increment, column reset and column increment, respectively) and generating 8-bit row- and column addresses as output, is needed. We don't think the reset address needs to be programmable at the moment. Could this address generator be a daughter card? Might it need a separate output cable?

Clock & bias voltages and currents

The APS sensor requires several bias voltages which, as in a conventional CCD, must be very quiet, and programmable, to obtain the best noise performance (e.g., VDD, VRST). Similarly, two clocks (PG and RST) probably require well-regulated levels. Although the absolute levels required by the APS are much lower than those used on a CCD (2-3 V vs 12-18 V), existing XIS driver board clock- and bias drivers appear to be more than adequate for APS needs for these signals.

On the other hand, there are two classes of signal that are not readily available from the existing driver board. First, at least three CMOS-level clocks, (SHR, SHS and CB, not counting the address generation signals described above) which do not require precise regulation, are needed. Second, two very quiet current sources (ICMN and ICMP) are needed. Although we don't know the details, the transistor dimension shown in Figure 3 of SV suggest that typical currents of about 50 and 250 μA are required for ICMN and ICMP, respectively. These currents control the active loads on various transistors in on-chip amplifier chain, so we would like them to be programmable so we can optimize performance. It is not clear to us how to generate these currents.

Questions: How can we augment the XIS driver to generate the required CMOS outputs and current sources? Can this be yet another daughter card?