High-Performance Active Pixel X-ray Sensors

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HIGH-PERFORMANCE ACTIVE PIXEL X-RAY SENSORS

1 Motivation

Future X-ray astronomy missions will be launched in pursuit of a variety of scientific objectives, and will entail technical advances on several fronts. While some of the most exciting new science will surely come from advances in cryogenic, non-dispersive spectroscopic detectors, megapixel imaging focal planes will be essential for the forseeable future. Progress in three major areas of imaging detector technology will be required in future missions: focal planes must be larger, mirror collecting areas must be greater, and soft X-ray (E $<$ 0.5 keV) detection efficiency will become increasingly important.

The focal plane area of the next generation of Explorer-class X-ray survey mission will likely exceed 150 cm^2, fully 4 times the 36 cm^2 active area of Chandra ACIS. Constellation-X will require over 400 cm^2 of detector area (total for four modules) for imaging and grating readout, and each focal plane module must service a telescope with ~ 4 times the collecting area of Chandra. Subsequent generations of X-ray observatories will require 10 to 50 times the focal plane area, and hundreds of times the collecting area of Chandra. The larger telescope collecting area raises the scientific value of good temporal resolution in the focal plane imager, and, for high-angular resolution optics, demands faster detectors to limit pileup.

A third trend in imaging detectors for X-ray astronomy is the increasing importance of soft (E $<$ 0.5 keV) X-ray response. Two factors drive this development. First, grating spectrographs offer the only practical technology that can provide the scientifically critical high resolving power ($E/\Delta E > 1000$) at energies below 1 keV. The multiple thermal blocking filters required by cryogenic microcalorimeter detectors seriously reduce detection efficiency below 1 keV, and the resolving power of these detectors falls linearly with energy. On the other hand, grating resolving power rises linearly with wavelength, and it turns out that the grating and its imaging detector comprise the spectrograph of choice for energies less than about 1 keV. Second, as larger collecting areas make it possible to probe the faint, high-redshift ($z > 3$) universe, key spectral diagnostic features, which are clustered at restframe energies E $<$ 2 keV, will be observed at $E < 0.5$ keV.

We propose to adapt an emerging imaging detector technology, that of the Active Pixel Sensor (APS), to the needs of X-ray astronomy. We believe this development is critical to the future of X-ray astronomy because current, ubiquitous, CCD-based imaging detector technology has serious inherent limitations that render it unsuitable for a variety of ambitious future missions. By virtue of its architecture, the APS overcomes these fundamental limitations of the CCD. For reasons we discuss in detail, however existing (bulk CMOS) commerical APS fabrication methods are incapable of producing useful X-ray sensors. We therefore propose to exploit a unique fabrication process, which we call Imaging/Silicon-on-Insulator, to produce highly-sensitive, low-noise X-ray imagers with APS architecture. In doing so we will take advantage of a multi-million dollar prior Government investment in this process at MIT Lincoln Laboratory. Our program will lead to X-ray imagers with all of the virtues of CCDs, but none of the signficant shortcomings. These sensors will dramatically improve the performance and reliability of future missions, while lowering instrument costs.

The plan of the proposal is as follows. After discussing the limitations of CCD imagers, we describe the APS architecture and show how it overcomes the limitations of CCDs. We then explain why commercial APS sensors are not suitable scientific X-ray imagers, and describe a new production process that allows us to incorporate the virtues of the X-ray CCD into a sensor with APS architecture. We conclude with descriptions of our research and management plans.

2 Limitations of CCDs

Charge-coupled devices (CCDs) have served as the principal focal plane detectors for every imaging X-ray astronomy mission launched dur-

ing the past ten years, and they are specified for a number of missions to be launched in the coming decade. CCDs have excellent quantum efficiency and can provide near-theoretical spectral resolution over the 0.3-10 keV spectral band. The ASCA, Chandra, XMM and HETE-2 missions have provided extensive flight experience with these detectors, and they must be regarded as a mature technology. Indeed, we have supplied CCD instruments for three of these missions (all but XMM) and the instrument we are currently developing for AstroE-2 is a third-generation design.

While CCDs are certain to remain detectors of choice for the very near-term, their limitations will become increasingly problematic for future missions. The most significant of these limitations are:

- The CCD is highly susceptible to degradation from on-orbit charged particle radiation.
- CCD focal plane readout times are long: of order seconds. This fact limits time resolution and leads to loss of science from pileup.
- The low-energy quantum efficiency of CCDs is reduced by the relatively thick optical blocking filters they require.
- CCDs require discrete analog and digital processors which are major consumers of instrument mass and power resources. Simply scaling the number of such processing systems with the focal plane area places impractical demands on these resources as pixel counts increase by an order of magnitude or more.

In the remainder of this section we discuss each of these limitations in detail.

Radiation damage. The CCD must transfer small charge packets (hundreds to thousands of electrons) extremely accurately (with losses of less than 1 part in 10^5 per pixel transferred) over distances comparable to the detector size (centimeters). Relatively small proton doses will seriously impair charge transfer efficiency and thus degrade spectral resolution and, particularly at low X-ray energies, detection efficiency. Indeed, since the radiation-induced fractional charge loss varies with event energy E roughly as $E^{-0.5}$, radiation damage is most problematic at low energies. Even for grating spectrographs, which rely on CCD energy resolution only for order separation, the loss of low-energy detection efficiency is thus a serious concern. CCD radiation damage has measurably affected the performance of all three of the imaging X-ray spectroscopy missions (ASCA, Chandra and XMM) in which they have been used. In fact, in their high-altitude orbits both Chandra and XMM rely on mechanisms to protect the detectors from soft (200 keV) protons which are focussed by the telescope.

Long readout times. The CCD has an inherently serial readout architecture, in which each pixel of the array must be sampled serially by one or at most a few parallel output amplifier/signal processing chains. For a given amplifier, noise requirements impose a lower limit on the processing time per pixel. This architecture leads directly to relatively long minimum readout times, typically of the order of seconds, in astronomical applications. In turn, these long frame times lead to event pileup and, via mechanisms described below, to enhanced sensitivity to noise from optical backgrounds and dark-current.

Poor low-energy quantum efficiency. A silicon X-ray CCD requires a blocking filter to reduce contamination from UV, visible and near-infrared radiation. For modern, back-illuminated detectors the blocking filter in fact determines the low-energy limit of the useful detector passband. The greater the optical density required, the greater soft X-ray attenuation of the blocking filter.

For a given level of contaminating out-of-band radiation, the optical density required in the blocking filter is determined by the speed with which the focal plane can be read, since the critical criterion is that the number of detected-out-

of-band photons per X-ray photon be sufficiently small (usually ~ 1.) Since the X-ray CCD integrates the out-of-band signal continuously during the exposure, (and can detect at most 1 X-ray photon per pixel per exposure if pileup is to be avoided) a longer frame time leads directly to a thicker blocking filter which, in turn, leads to poorer low-energy X-ray sensitivity. Conversely, if the focal plane readout time can be reduced, the optical density of the blocking filter can be reduced, and the soft X-ray efficiency of the detector can be increased.

The resulting improvement in soft x-ray response can be quite dramatic. For example, if the readout rate of the CCDs on the XMM/RGS spectrograph could be increased by a factor of $\sim 10^3$, which, we shall argue, is well within the capability of technology we propose to develop, then no blocking filter would be required at all! The system detection efficiency at 200 eV would be improved in this case by a factor greater than two. The expected improvements in quantum efficiency for a direct imager (modelled after Chandra ACIS-S) and for the RGS case are illustrated in Figure 1.

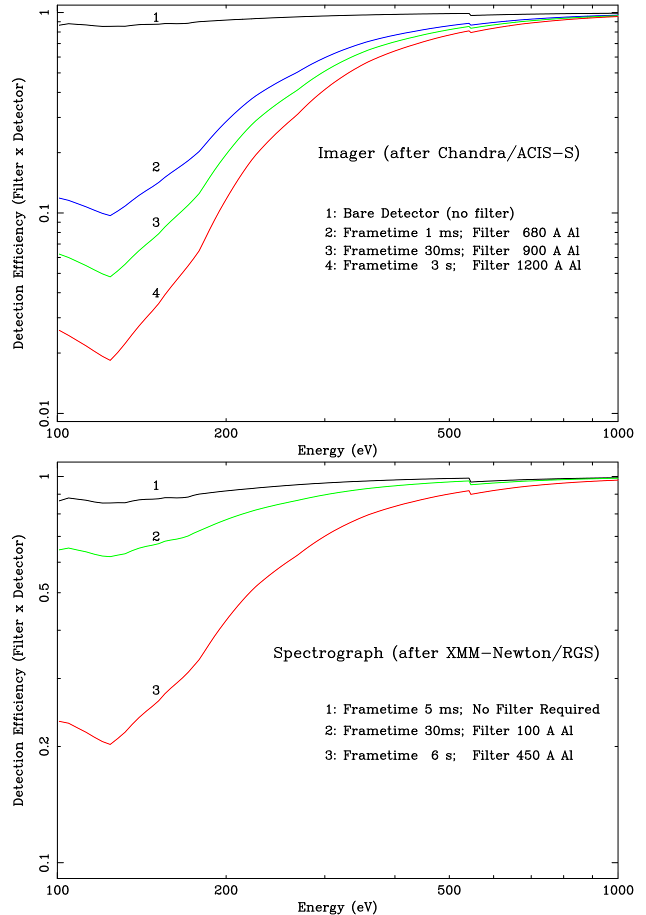

Figure 1: **Faster readout improves low-energy quantum efficiency** for X-ray photon counting detectors because the contaminating out-of-band signal per X-ray photon is proportional to the frame time. The required physical thickness of the blocking filter is a linear function of the logarithm of the frame time. The detection efficiency gain is greatest at the lowest energies. Thus, the higher parallelism afforded by active pixel sensors offers dramatic improvements in low-energy quantum efficiency. **Top:** Improvement expected for a broadband imager, scaled from the Chandra/ACIS-S. **Bottom:** Improvement expected for a grating spectrometer detector, scaled from the soft X-ray detectors on the XMM/RGS, which see a lower contaminating optical flux. In this case, if a frame time less than about 5 ms could be achieved, in principal no blocking filter would be required at all.

Signal- and data-processor scaling. As focal planes grow larger, demands on analog and digital signal processing increase. If the focal plane readout time is not to increase then the required processing throughput scales linearly with the area of the focal plane. Since the pixel rate per channel is limited by the need to minimize readout noise, a larger CCD focal plane implies a larger number of parallel processing channels. In existing instruments, these parallel processing channels account for a large fraction of the mass (e.g., 2/3 of the total instrument mass in the case of Chandra/ACIS) and for an even larger fraction of the power consumed (about 85% of the power in the case of ACIS.) It is simply impractical to replicate the number of such processing chains to accomodate increases in focal plane area of an order-of-magnitude or more.

One obvious approach to this problem is to develop application-specific integrated circuits that provide highly parallel processing channels. While this may be feasible for the very largest

missions, in general the development of space-qualified, low-noise analog signal processors that are matched to the output characteristics of a particular detector will be beyond the budget of any particular instrument. Integration of these functions on the CCD detector wafer itself is in general problematic, because conventional CCD fabrication technology (usually bulk NMOS) is incompatible with the CMOS technology used to produce modern, high-density, low power circuits.

3 Active Pixel Sensors

To overcome the limitations of CCDs, we propose here to develop an alternative sensor architecture, that of the Active Pixel Sensor (APS), for use in high-performance, photon-counting X-ray imagers. The readout architecture of the APS addresses all of the limitations of the CCD which we have discussed above: an APS will tolerate many orders of magnitude more non-ionizing radiation than will a CCD, it is capable of much shorter frame times, it requires much thinner optical blocking filters (in some cases no optical blocking filter at all!) so it is more sensitive in the crucial E $<$ 0.5 keV band, and, since it is easily integrated with digital processing, it can be readily used in very large focal planes.

Despite the virtues of its architecture, however, APS as now commercially fabricated, with standard CMOS technology, are not suitable for use as scientific X-ray sensors. There are two principal limitations of commercial APS. First, the typical readout noise ($> 50e^-$ RMS) is at least an order of magnitude higher than is required for scientific applications. Quiet ($\sim 5e^-$ RMS noise) sensors have been built and operated in the laboratory [1] however, so high noise is not inherent in APS architecture. The high noise of commerical APS probably reflects the particular requirements of their commercial applications. Second, the CMOS fabrication technology used to make APS is incapable of producing photosensitive volumes which are thick enough to detect soft X-rays efficiently. Generally the photosensitive regions in CMOS sensors are less than 1μm thick; typical X-ray CCDs have photosensitive thicknesses of order 50μm. This limitation is inherent in standard CMOS fabrication technology. There is therefore very little prospect that commerical APS producers will ever develop an X-ray detector of scientific interest.

We propose to exploit a novel "Imaging/Silicon-on-Insulator" (I/SOI) fabrication process developed at MIT Lincoln Laboratory to produce low-noise, high-performance active pixel X-ray sensors. We will demonstrate that this technology allows us to combine the virtues of the deep-depletion, low-noise CCDs we have produced for ASCA, Chandra, Astro-E and HETE2 with the advantages of the APS architecture. In the remainder of this section we describe the APS architecture, explain how it addresses the inherent limitations of the CCD, examine the deficiencies of commercial APS in greater detail and then explain how the sensors we propose would overcome them. In Section 4 we describe the I/SOI fabrication process, and show how it can be used to make high-performance, X-ray sensitive APS. We describe our research goals and plans Sections 5 and 6.

3.1 APS Architecture

APS and CCD architectures are fundamentally different. The APS layout, illustrated schematically in Figure 2, is similar in some respects to that of a random access memory. In contrast to the CCD, each APS pixel is directly addressable, in the sense that APS pixels can be read in any sequence. This is possible because each pixel includes not only a charge collection node, which can integrate photon-induced signal, but also dedicated transistors that perform charge-to-voltage conversion, pre-amplification and reset. The outputs of the pixel amplifiers in each column are connected through a row selecting switch to a vertical bus which carries signal to column readout circuitry. Typically an entire row of pixels can be read out simultaneously into the column buffers. Readout of the entire frame is accomplished by reading each row sequentially. Thus, in a 1000x1000 pixel device, up to 1000 channels can be read in parallel. Provided that

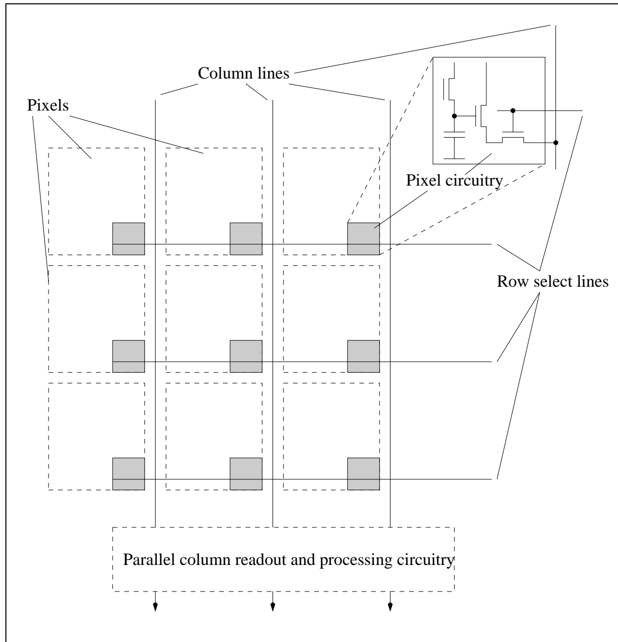

Figure 2: **The Active Pixel Sensor architecture allows parallel rather than serial readout.** All pixels in a row can be read simultaneously, so much higher frame rates can be achieved than are possible with CCDs. Moreover, the amplifier circuitry in each pixel eliminates the need for charge transfer, so the non-ionizing radiation tolerance of an APS is several orders of magnitude better than that of a CCD.

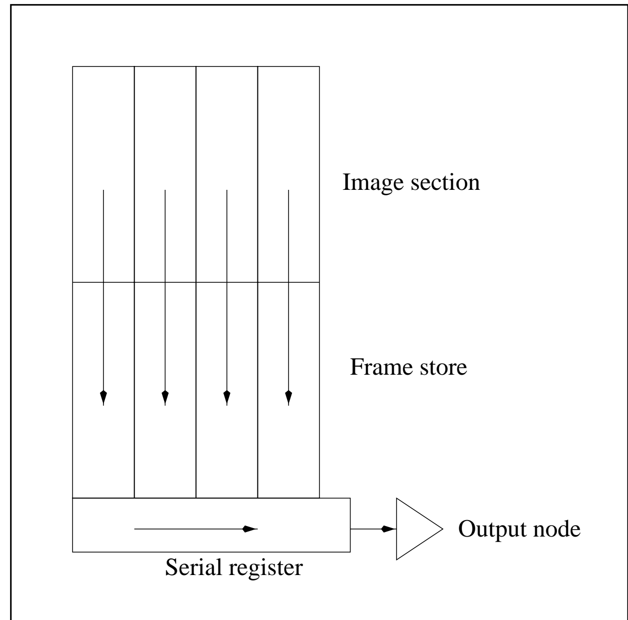

Figure 3: **CCD architecture requires serial readout** of every pixel, and therefore is limited to much lower frame rates than are possible with APS. Moreover, the long-distance charge transfer required makes the CCD very susceptible to radiation damage.

the output circuitry contains a processing channel for each column, the frame time is the product of the number of rows in the device and the time required to read and process a single pixel.

In contrast, the CCD architecture, illustrated in Figure 3, is inherently serial. Each column of the CCD is a "vertical" serial shift register, and each such column feeds a single element of a "horizontal" output serial shift register. An amplifier at the end of the output register converts each charge packet in turn into an electrical signal. During readout, after rapidly transferring the signal from image to the framestore section, (an operation which demands high peak power) the vertical registers are shifted once to load a row of charge into the output register, and then each pixel in the output register is readout serially. Only after every pixel in the output register has been read can the cycle be repeated to readout the next line. The total frame time is thus the product of the number of pixels in the array and the time required to process a single pixel. In practice, segmented output registers with multiple output transistors allow modest parallelism (two outputs per device in the case of XMM/EPIC/MOS, or four outputs per device in the case of Chandra/ACIS, for example), but, for a given pixel readout time, the CCD frame time will exceed that of an APS by a factor equal to (one-half or one-quarter of) the number of pixels in a row, i.e. by a factor of order 100-1000.

The column-parallel architecture of the APS, and the very small CMOS transistors now available (with feature sizes as small as $\sim 0.15\mu$m) together make highly parallel signal processing possible. Such processing can be quite complex and may include Correlated Double Sampling (CDS) and Analog-to-Digital Conversion (ADC). One recently announced device [2], for example, is a 4 megapixel imager with more than 2000 10-bit ADC's on-chip. This highly parallel architecture delivers 1 Gpixel/s (240 frames/sec)

from an input power of only 700 mW.

In addition, the APS's random-access capability provides a great deal of flexibility in focal plane readout. In principle, different regions of the focal plane can be readout at different rates, so, for example, regions surrouding a known bright source could be readout extremely rapidly while the remainder of the field is readout more slowly.

3.2 Advantages of APS

Active pixel sensors address all of the limitations of CCDs outlined in Section 2, and have some other very significant advantages as well. In this section we discuss these advantages in greater detail.

Much better radiation tolerance. Charge transfer distances in an APS are less than the size of a single pixel, which is to say they are typically 1000 times shorter than in a CCD. In consequence, the APS tolerance for non-ionizing radiation encountered on-orbit, the Achilles' heel of the CCD, exceeds that of the CCD by orders of magnitude. Therefore, the useful life of an APS sensor will far exceed that of a CCD. Moreover, the massive shielding required by CCDs (typically 10 gm cm^{-2} aluminum equivalent over most of the sphere) is not required by an APS instrument. Not only will this weight saving be especially important for very large focal planes, but the reduced mass in close proximity to the detector will probably lead to lower particle-induced background as well. We note also that the improved radiation tolerance will lead to a more stable calibraton over the mission lifetime, and therefore will reduce operations costs.

The tolerance of APS for ionizing dose can be made very large (over 100's of krad Si), especially using the I/SOI technology we propose [3]. The oxide layer used in this process is a factor of three thinner than that used in standard CCD fabrication, so the sensitivity to threshold shifts due to ionizing dose will be correspondingly smaller. At the dose levels expected in typical on-orbit environments we do not expect any significant radiation degradation in transistor characteristics. Moreover, the CMOS structures produced by our I/SOI process are immune to the conventional latchup phenomenon which can affect bulk CMOS devices because carriers created in the bulk of the wafer by energetic particles cannot flow into the active circuits (see Section 4, below).

The dominant effect of radiation on APS sensors is likely to be an increase in dark current arising from the ionizing dose. The specific susceptibility (change in dark current density per unit ionizing dose) of an I/SOI APS will be comparable to that of a CCD. The contaminating dark current signal is proportional to frame time, however, so the APS tolerance for ionizing dose at a given detector operating temperature will be greater than that of the CCD by the inverse of the ratio of the frame times, that is, by a factor of 100 to 1000. In practice, some of this margin could be used to raise the detector operating temperature. We discuss this point more fully in the following paragraphs.

Much shorter readout times. Perhaps the most significant scientific performance benefit of the factor of ~ 1000 reduction in frame time provided by APS is the improvement in low-energy quantum efficiency. This was illustrated in Figure 1, which shows that for applications in which the optical flux is comparable to that of the Reflection Grating Spectrometer on XMM, an APS with a 1 ms frame time would not require any blocking filter at all. (In fact, no filter is required for frame times less than about 5 ms.) The result is a factor of almost three increase in effective area below 200 eV, compared with the RGS CCD. As noted in Section 2, even for a direct imager, which generally must contend with higher levels of optical contamination than a grating spectrograph, one would expect at least a factor of 2 increase in effective area at 200 eV. *These detector improvements have extremely high scientific leverage:* they would enable the 4-spacecraft Constellation-X mission, for example, to study the critical OVII and OVIII lines of sources at redshift z=3 with the power of twelve spacecraft equipped with conventional CCDs.

A second direct scientific advantage of the vastly shorter APS frame time is the factor of ~ 1000 improvement in time resolution. This ca-

pability will maximize the scientific return from planned future imaging missions with collecting areas approaching or even exceeding that of XTE.

Another scientific benefit of the APS's shorter frame time is a reduction in pileup. Pileup occurs in an X-ray photon-counting imager when two photons interact within a single pixel (or in adjacent pixels) within a single exposure. Obviously, the APS can observe much brighter sources without event pileup than can a CCD. This capability will be most significant for very high-angular resolution missions. Were the proposed Generation-X mission, with collecting area of order 10^2 m^2, and image size of order $1''$, to use CCDs with frame times of order 1 s, for example, pileup would be severe for *any* source detectable in the deepest ROSAT survey fields. In fact, for Generation-X, the pileup fraction would exceed 10% for sources with $f_X >\sim 3 \times 10^{-15}$ erg s^{-1} cm^{-2}.

Finally, there is a very important engineering advantage arising from the shorter APS frame time: the operating temperature can be increased significantly. Conventional photon-counting X-ray CCD operating temperatures range from -60C (ASCA) to -120C (Chandra) and are driven by two requirements. First, dark current must be suppressed, and second, a CCDs susceptibility to the effects of radiation-induced displacement damage is generally minimized at lower temperature. The contaminating dark current signal is superficially similar to that produced by contaminating optical radiation, although since the mean dark signal can usually be measured and subtracted onboard, it is the noise in the dark current that is the chief concern. When the mean dark signal, in electrons per pixel per frame time, equals the amplifier noise variance, the dark current begins to dominate the system noise. Since the origin of the dark current is thermal excitation, the dark signal can be reduced by lowering the detector operating temperature. The dark current rate increases with exposure to ionizing radiation, and the detector operating temperature range must be chosen to provide acceptably low dark current at the end of mission. ASCA experience [4], for example, sugggests that the radiation-induced dark current increase observed after 5 years on orbit could have been suppressed to the (negligible) pre-launch levels by a reduction in detector temperature of about 15C.

Since the contaminating dark current signal is proportional to the frame time, APS sensors will effectively have lower dark current than conventional CCDs. The effect of reducing the frame time on the dark signal is illustrated in Figure 4. The Figure shows, for example that a back-illuminated APS sensor with 24 μm pixels and a frame time of 1 ms could thus operate with less than 1 electron per pixel per read at a temperature of about -12C, nearly 60C warmer than a CCD with equivalent dark current signal per read. This capability leads to an enormous simplification in thermal system design. Even allowing for a 15C margin to accomodate radiation-induced dark current, for example, a -30C focal plane temperature could be readily achieved using passive focal plane cooling even in low-earth orbit. The complexity and power consumption of Peltier cooling would no longer be required. This advantage becomes increasingly important as focal planes grow larger and thermal loads increase. Moreover, the much lower temperature difference between assembly/storage and operating temperatures will improve reliability.

Readily scalable signal- and data-processing. The integrated CMOS circuitry and the "random access" architecture of the APS sensor allow compact, low-power integrated processing capability to be incorporated in the sensor design. This enables the operation of very large focal planes at high frame rates within a reasonable power budget.

Column-parallel analog signal chains, including A-to-D converters, can be readily integrated on chip. This integration reduces the capacitive loads in the signal processing chains, which both lowers power consumption and, in principle, improves noise performance. The feasibility of massively parallel, on-chip signal chains has been demonstrated: CMOS imagers with over two thousand on-chip A-to-D converters are commercially available that collectively digitize over 10^9 pixels s^{-1} with a power consumption of

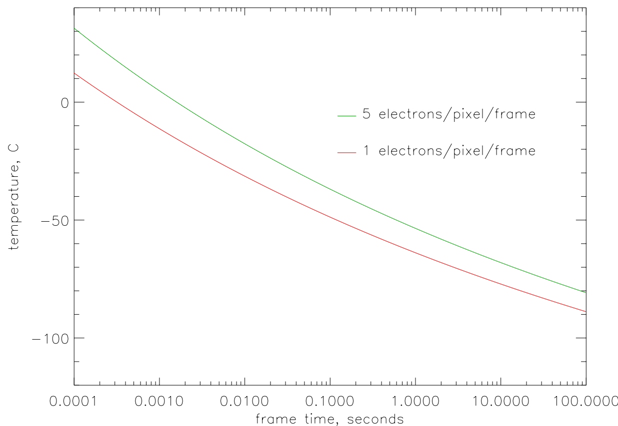

Figure 4: **The much shorter APS frametime allows significantly higher detector operating temperature.** The estimated temperature required to achieve a given dark signal level is shown as a function of frametime. A typical CCD frametime is a few seconds, while a typical APS frametime $\sim$ 1ms, so the APS requires much less cooling than a CCD. A back-illuminated sensor with 24-μm square pixels has been assumed.

700 mW [2]. As we discuss in Section 6 below, we believe the flexibility of the APS architecture may allow us to exploit the very sparse characteristics of X-ray data, and, by identifying X-ray events on-chip, to reduce the data rate to the remainder of the instrument (and the processing throughput required of it) by orders of magnitude.

Other Potential Advantages The APS technology we propose offers a number of other potential advantages over CCDs. We list these briefly here:
Lower noise: As we discuss below in Section 6.2.1 and illustrate below in Figure 10, the very small sense transistors of our I/SOI process will have much lower capacitance, and therefore potentially much lower noise, than conventional CCD on-chip amplifiers.
No frame transfer: Conventional X-ray CCDs are frame-transfer devices. The image-to-framestore operation must be done quickly to minimize image streaking, and therefore requires high peak power. The framestore area occupies useful focal plane real estate, and also increases the effective exposure time, thereby increasing the contaminating signal from both charged-particle background and dark current.

3.3 Overcoming Limitations of Existing APS

Conventional CMOS APS have a number of limitations which render them unsuitable for use as scientific X-ray sensors. In this section we discuss these limitations and indicate how our approach overcomes them.

Correlated Double Sampling for Low Noise. Commercially available APS have very high noise levels, typically 50 e^- or more. The main component of this noise is the kTC noise of the integrating photodiode, which has to be reset before every integration cycle. In a CCD, kTC noise is removed by correlated double-sampling (CDS) circuitry, which is part of the off-chip signal processing chains. In an APS with a photodiode pixel, which is by far the most common choice for commerical APS due to its good blue sensitivity, CDS is difficult to implement.

Our approach is to provide for CDS processing circuitry. Details of the pixel design, as well as our approach to correlated double sampling, are discussed in Sections 6.1.1 and 6.2.1 below.

I/SOI for X-ray Sensitivity. Commerical bulk CMOS APS sensors have depleted photosensitive volumes which are only $0.2 - -0.5\mu$m thick, a factor of 100 thinner than state-of-the-art silicon CCDs. The reasons for this, as well as means by which our proposed I/SOI fabrication technology overcomes this limitation, are described in Section 4 below.

Fixed Pattern Noise. Another limitation often attributed to APS is fixed pattern noise (FPN), which is produced by a variety of mechanisms, including dark current nonuniformity and variations of transistor geometry in pixels and signal readout chains. It is becoming common to correct for these non-uniformities with additional on-chip circuitry, or to compensate for them digitally using bias maps. Our approach eliminates FPN caused by different offsets in the pixel and readout circuit using correlated dou-

ble sampling. As with CCDs, the contribution of dark current to FPN in our sensors will be eliminated by choice of operating temperature (though, as discussed in Section 3.2 above, an APS poses much less stringent operating requirements than would a CCD.) In astrophysical applications where extremely high accuracy of measurement is very important, digital frame bias maps are commonly used for CCD detectors and in case of APS they will also provide an adequate way to suppress FPN. APS sensors may require responsivity maps as well, since each pixel will contain a distinct charge-sensing transistor. Similar corrections are routinely used for imaging infrared sensors. We note that this processing could very likely be performed on-chip. The required *calibration* of these responsivity variations will be straightforward since, because of its high frame rate, the APS sensor is capable of acquiring X-ray calibration data at a much higher rate than is possible with a CCD.

Fill Factor. In APS part of each pixel is occupied by transistor circuitry, so the photosensitive area has a "fill-factor" less than 100% if the device is used in a front-illuminated configuration. Our approach addresses this limitation in two ways. First, for reasons detailed in Section 4, our Imaging-SOI technology allows for much smaller transitors than does standard CMOS processing, so the fill-factor of a front-illuminated device will be much better than for conventional CMOS APS sensors. Indeed, we would expect a fill factor of at least 85% in a typical 24 μm-pixel. Moreover, SOI devices are very thin, so even the obscured areas would be expected to be senstive at X-ray energies above 1 keV. However, for both APS and CCDs, maximum quantum efficiency, especially at low energies, requires back-illumination. Our proposed sensor is fully compatible with state-of-the art back-illumination treatment, as we discuss in Section 4 below. In a back-illuminated configuration, the APS we propose would have effectively 100% fill-factor.

Non-CMOS APS. There exists a type of detector whose architecture is rather similar to that of an APS, the so-called DEPFET [22]. The device is based on pn-CCD technology developed at the Max Planck Institute in Germany and utilizes JFET transistors. While promising early noise results from these devices have been reported [23], the pixel size is quite large (50×50 μm), and cannot easily be reduced with this architecture. DEPFET technology does not include CMOS (or even MOS) circuitry and this makes any on-chip signal processing virtually impossible. Therefore the sensor requires several dedicated supporting chips for array control and signal readout and processing. Moreover, this device requires very high controlling voltages (about 25 V). As a result power consumption is comparable to that of a CCD with off-chip processing circuits. The need to control every row and every column with a separate bonding wire severely limits number of pixels; the largest array size is currently 64x64.

We believe that a much more promising and flexible approach for future missions is to incorporate the best characteristics of CCD detectors in a sensor with APS architecture and CMOS processing capability. In the next section, we describe the MIT Lincoln Laboratory I/SOI fabrication process which makes this synthesis possible.

4 The Imaging/SOI Fabrication Process

In order to realize the advantages of APS in a high-performance X-ray sensor, we propose to exploit a unique "Imaging/Silicon-on-Insulator" (I/SOI) fabrication technology recently developed at MIT Lincoln Laboratory. This process is uniquely suited to the production of high-sensitivity, low noise solid- state X-ray detectors with all of the advantages of the APS architecture. In this section we discuss the merits of SOI fabrication, and then describe the unique features of the MIT/Lincoln Laboratory I/SOI process.

SOI wafers employ a buried silicon dioxide layer (BOX) to separate a thin silicon layer from the mechanical support of the bulk silicon wafer. Figure 5 contrasts the structure of SOI-based transistors to those fabricated in conventional

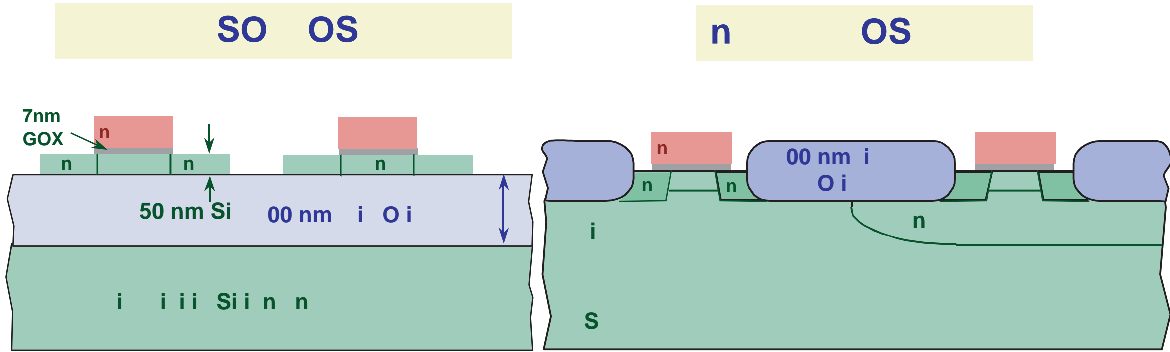

Figure 5: **Schematic cross-section of CMOS transistors fabricated on our proposed, fully depleted I/SOI process (left) with those made in a conventional n-Well bulk CMOS process(right).** I/SOI transistors are smaller, have lower capacitance and power consumption, and potentially lower noise when compared to bulk CMOS transistors. Most importantly, I/SOI allows for the integration CMOS active elements in deep-depletion X-ray sensors.

bulk technology.

Devices fabricated in SOI benefit from reduced parasitic junction capacitances and suppressed short channel effects due to the presence of the insulator beneath the devices. The fully depleted (FDSOI) operating mode created by a 0.05 μm (50 nm) silicon active layer offers further advantages with its reduced channel capacitance, enhanced subthreshold swing, and minimized floating-body effects, when compared to a more conventional partially depleted (PDSOI) technology. These inherent advantages in the FDSOI structure offer lower power consumption and, as we shall show below, potential reductions in noise, compared to conventional technologies. We have demonstrated these power savings by fabricating 0.25 μm FDSOI ring oscillator devices for which we measure delays of 25ps at 2V. Corresponding bulk silicon circuits consumed five times more power for the same speed performance.

As is illustrated in Figure 5, the SOI process uses discrete islands for transistors instead of the traditional bulk local oxidation (LOCOS). This simplifies the device isolation process and achieves high device layout densities. Moreover, because there is no need for junction isolation between devices, FDSOI CMOS does not suffer from the bipolar latchup condition that can arise in bulk devices exposed to ionizing radiation.

Indeed, radiation hardness in SOI CMOS is improved over bulk CMOS because of the reduced volume of silicon used by the transistors and since carriers created in the bulk wafer by energetic particles cannot flow into the active circuits. SOI circuits have also been shown to be less prone to single-event-upset damage than bulk CMOS technologies [18]. To minimize the radiation-induced threshold reduction and leakage current increase seen in nMOSFETs, the BOX can be treated [19, 21] to compensate the induced positive charge build-up. We have incorporated treated SOI material with our 0.25 μm and 0.18 μm FDSOI processes and have observed improved tolerances up to X-ray doses of 1Mrad (SiO2) [3].

While the SOI layer can yield high-speed, low-power, radiation-tolerant transistors, ordinary SOI does share one limitation with conventional CMOS fabrication discussed above in Section 3.3. The silicon layer is much too thin (0.05 μm) to provide useful X-ray photon absorption. Our I/SOI process technology removes this limitation. We take advantage of the BOX separation between the transistor layer and the support wafer and use the support wafer for high-sensitivity photodetection. The implementation of a photogate APS pixel design (as discussed above in Section 3.1) is illustrated schematically in Figure 6. The detector elements are fabricated

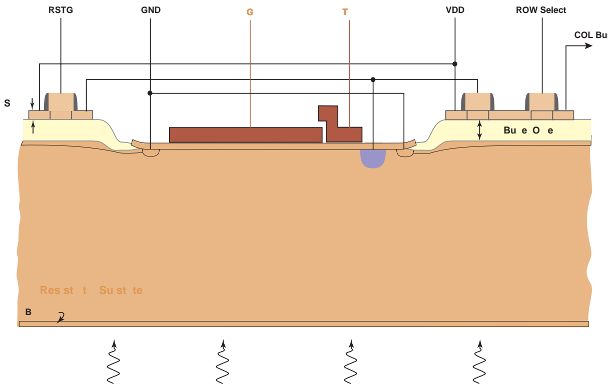

Figure 6: **Our proposed I/SOI process produces APS sensors with the deep depletion required for efficient X-ray detection.** This schematic shows a back-illuminated, photogate pixel design on a high-resistivity silicon substrate. The drawing is *not* to scale. With proper bias on the photogate (PG), depletion depths comparable to modern X-ray CCDs (50 μm or more) can be achieved. For clarity, the area occupied by the SOI transistors is greatly exagerated. For a 24 μm pixel, the SOI structure would occupy less than 15% of the pixel area.

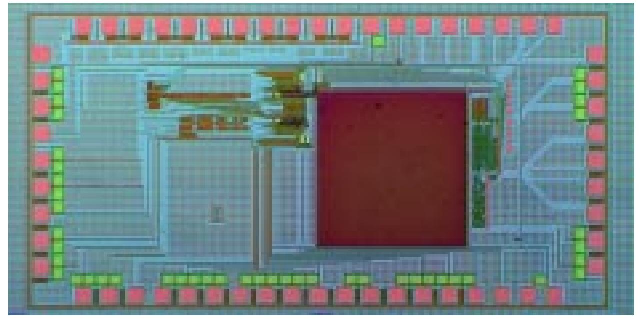

Figure 7: **Proof of the I/SOI concept's feasibility was demonstrated** with this integrated 128x128 pixel CCD with CMOS on-chip clock generation and A-D conversion. Excellent imaging performance was achieved.

in the bulk high-resistivity wafer and the reset, amplification, and access transistors are fabricated in the thin SOI layer.

A crucial advantage of I/SOI is that we are able to achieve large depletion depths necessary for efficient X-ray detection. In early demonstration of of enhanced depletion depth, an APS produced on 300 Ω-cm silicon in our facility demonstrated dramatically improved spectral response in the visible and near-infrared, compared to a bulk CMOS design [5]. Using a 3.3V, 0.35 μm gate length version of this process, we have also demonstrated a CCD image sensor with on-chip clocking and analog-to-digital conversion on 300 Ω-cm silicon [6]. This device is illustrated in Figure 7.

We note that the deep depletion depths we require simply cannot be achieved with conventional, single-well bulk CMOS fabrication technology, even if high-resistivity silicon were used. The bulk CMOS photodiode structures are restricted to implant combinations used in transistor fabrication: n+(source implantation)/p-substrate, nwell/psubstrate, and p+(source implantation)/n-well/p-substrate. The extent of the photoconversion region in bulk CMOS imagers is thus constrained by the shallow junctions, the narrow epitaxial silicon layer thickness, and the high well dopings required for submicron digital circuits. Typical bulk CMOS depletion depths of 0.2-0.5 μm are much too small for X-ray detection. Current generation X-ray CCD sensors, for example, exhibit depletion depths between 30 and 75 μm.

The buried oxide isolation between SOI transistors and the photosensitive devices in our I/SOI process also preserves the integrity of signal charge collection without corruption from the readout electronics. In contrast, bulk CMOS APS are sensitive to spurious charge injection from high field regions in CMOS junctions, to stress-induced defects arising from the shallow trench and LOCOS (local isolation) processes, and to dark current generation from silicided regions. Process-induced crystalline dislocations are another potential source of dark current in bulk CMOS APS. For the Chandra/ACIS instrument, we developed slip control procedures to guard the fragile high resistivity wafers from dislocation generation during fabrication [7] and special anneals to assure complete defect passivation. These methods have also been implemented in our I/SOI technology. We have observed neither slip dislocations nor other adverse effects when subjecting a test CCD lot (fabricated in the 3000 Ω-cm SOI handle wafer) to

rapid thermal annealing (RTA) cycling imperative for submicron CMOS formation [8].

Back illumination is a critically important component of soft-x-ray detectors for E < 1 keV, whether CCD or APS. Although back illumination of the APS wafers is not part of this proposal, we note that the I/SOI APS wafers we build will be fully compatible with our back-illumination process. Recently, MIT Lincoln Laboratory has developed a back-illumination process whose UV performance suggests high quantum efficiency at all soft-x-ray energies. This process is now used routinely on large-area CCDs for astronomy, and the yield and cosmetic quality are substantially superior to an earlier process used on the Chandra back-illuminated devices [14]. In the new process [17] the wafer is thinned to a free-standing membrane with a narrow, unthinned rim to allow handling, and a boron-doped Si layer, about 5 nm thick, is grown on the etched surface using molecular beam epitaxy (MBE.) This p+ layer provides the necessary electrical barrier to photoelectrons to prevent recombination losses at the back surface. As optical detectors these MBE-treated devices exhibit 100% internal quantum efficiency (QE) in the ultra-violet from 200 to 850 nm. From 200 to 400 nm the absorption depth in silicon is as small as 5 nm, so any dead layer must be extremely thin. Since the absorption lengths in this portion of the spectrum are even shallower than in the soft-x-ray regime we believe that such devices will have great promise at energies below 1 keV.

MIT Lincoln Laboratory has been building complex, low-voltage CMOS integrated circuits in FDSOI [9] since 1995 under DARPA's Low Power Electronics and Advanced Microelectronics programs. We also perform multiproject fabrication, with 120 separate designs completed to date for 30 different organizations in industry, government, and academia. The core technology has evolved from the initial 0.25 μm minimum dimensions to the present 0.18 μm for large circuits and sub-0.1 μm for experimental efforts, and has been extended to applications in imaging, radar, and electronic intelligence. All of our fabrication work is done in Lincoln's Microelectronics Laboratory, a modern, fully-equipped facility described in greater detail in the Appendix. Here we note that Lincoln's captive fabrication capability permits fine tailoring of process parameters (such as dopant position and concentration) to optimize device performance characteristics (such as dark current, photogenerated carrier collection, and noise.) This flexibility is essential to our proposed development program.

MIT Lincoln Laboratory is actively supporting further development of the I/SOI process through Internal Research and Development funding. As part of this effort, a research I/SOI lot is currently in fabrication. We propose to exploit this lot, which for convenience we label the "Development Lot," in the first phase of our effort to develop high-performance APS for X-ray astronomy. Development Lot fabrication will be completed before the end of calendar year 2002. The lot includes fabrication steps to selectively expose, pattern, and dope regions of the bulk silicon support wafer, thereby creating photosensitive devices in submicrometer-scale proximity to the FDSOI transistors. Two Development Lot test devices are especially relevant to the development of high-performance X-ray APS. We describe these devices, what we hope to learn from them, and the rest of our proposed research plan in Section 6 below.

Our proposed effort leverages the enormous investment DOD has made in this technology over the past 7 years. The design and production of the Development Lot alone represents a DOD investment of over one million dollars.

5 Research Goals

We propose a three-step, three-year research program with the goal of demonstrating that a high-frame-rate, low-noise, deep-depletion Active Pixel X-ray imager is feasible. Our performance goals are listed in Table 1, and may be summarized as follows. We wish to demonstrate a noise level of < 3 e$^-$, RMS) at rates of at least 10^6 pixels s^{-1} per column. In order to ensure that a sufficient number of test and process assessment structures can be included in the die, the demonstration devices we build will have a

512 × 512 pixel format. There is no reason, in principle, why larger-format devices could not be built in later production lots.

We will implement correlated double sampling so that analog signal processing for all columns can proceed in parallel. While we will include prototype A/D designs on our demonstration devices, for reasons we describe in Section 6.2.3, we do not plan to implement full, column-parallel A/D conversion on these sensors. We note that our target pixel rate corresponds to a frame-rate of 1000 frames s^{-1} in a megapixel imager with full column-parallel processing.

We will demonstrate depletion depths comparable to or better than state-of-the art X-ray CCDs ($\sim 50\mu$m). We further aim to demonstrate an X-ray-sensitive APS with a tolerance for non-ionizing radiation which is at least 1000 times better than that of current-generation CCDs, and which achieves these performance levels at an operating temperature warmer than -25C.

The devices we fabricate will be fully functional front-illuminated X-ray imagers. While we do not propose here to build back-illuminated sensors, the wafers we fabricate would be ready to receive the MBE backside treatment described above in Section 4 in a follow-on program.

6 Technical Approach

To achieve these goals, we propose to accomplish three major tasks. First, we will conduct a comprehensive test program to characterize noise and power consumption in I/SOI CMOS sense transistors and performance characteristics of APS sensors now being fabricated in the (already-funded) Development Lot. Second, we will investigate alternative architectures for a next-generation APS X-ray sensor. This investigation will rely on the test results obtained in Task 1, and will address three specific topics: noise minimization through optimum transistor- and pixel design, charge collection modelling to ensure good X-ray detection efficiency and spectral response, and optimum integration of digital processing into the APS sensor. Our final task will be to design, fabricate and test a next-generation Active Pixel X-ray imager. This device will incorporate all we have learned in Tasks 1 and 2. In the following sections we describe each of these tasks in greater detail.

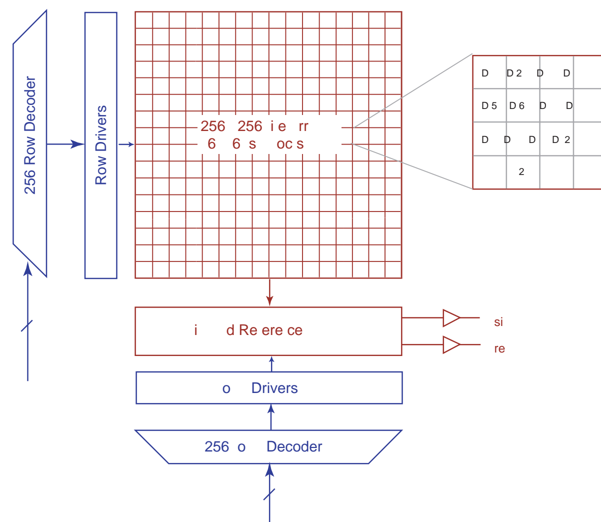

Figure 8: **Schematic block diagram of the I/SOI "Development Lot" Active Pixel imager we will evaluate as part of Task 1.**

6.1 Task 1: Characterization of Development Lot Devices

This task is devoted to characterization of two devices currently in fabrication in the Development Lot. The devices, test objectives and the tests we propose are described in detail in the following sections.

6.1.1 I/SOI Active Pixel test imager

The Development Lot contains an APS process evaluation device which we will characterize in order to understand critical process and design improvements required to realize a high-performance X-ray APS. This 256x256 pixel SOI-CMOS APS imager, shown schematically in Figures 8 and 9, contains sixteen subarrays, each containing variation in pixel layout and detector doping profile. The array includes both photodiode (PD) and photogate (PG) pixels. In a PD pixel, charge is integrated onto a depleted n+/p junction that also serves as the floating diffusion

Parameter	Goal for Demonstration APS	Typical CCD
Read Noise (e^{-1}, RMS)	< 3	3
Pixel Rate (pixels s^{-1})	$\geq 10^6$	$< 10^5$
Equivalent Frame Rate* (fr s^{-1})	$\geq 10^3$	0.3
Depletion Depth (μm)	> 50	50
Non-ionizing Radiation Tolerance (relative)	1000	1
Operating Temperature† (°C, post-irradiation)	-15 to -25	-80 to -120

*For a 1 Megapixel imager. Demonstration device will have 512×512 pixels.

†After 1 krad (Si) ionizing dose, with dark current < 1 e^{-1} pixel per readtime.

Table 1: Performance goals for the I/SOI Active Pixel Demonstration Sensor

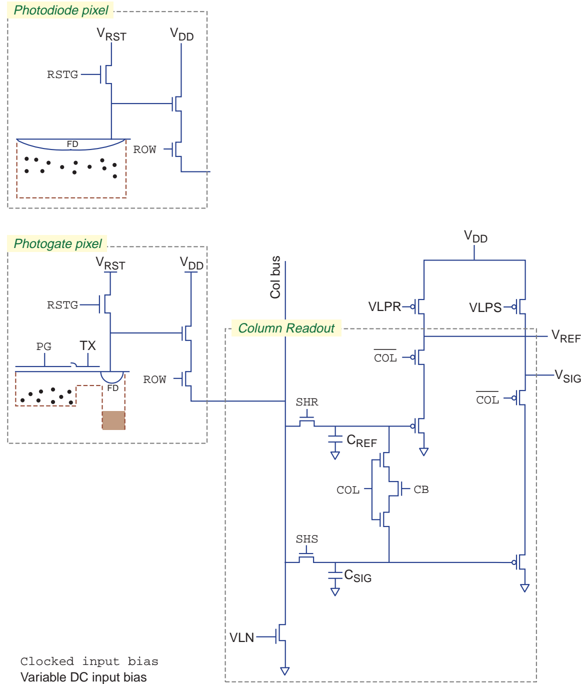

Figure 9: **Pixel and readout multiplexer designs in the I/SOI "Development Lot" Active Pixel imager we will evaluate as part of Task 1.**

(FD) node. At the end of the integration time, the charge signal is read out and then the junction is reset using the in-pixel reset transistor RSTG. In the PG pixel, charges are integrated under the PG biased at 3.3V. The transfer gate (TX) isolates the integration area from the sense node and is biased at a constant intermediate voltage. The FD node is reset with RSTG and at the end of the integration period the photosignal is transferred from the collection area into the FD sense node. Each pixel thus contains a photodetector, a source follower input transistor, a row-selection transistor, and a reset transistor. The photogate pixels also include a transfer gate to move charge from the integrating capacitor onto the sense node. The photodetector is fabricated in the bulk high-resistivity support wafer with all transistors fabricated as body-tied FD-SOI nMOS to minimize floating body effects and (potentially) noise. Variations in photodetector doping layout are explored to evaluate differences in junction depth, charge collection, conversion gain, and fill factor. The peripheral circuits are row and column decoders, row buffers, and sample-and-hold circuits. This test sensor employs a commonly used correlated-double-sampling (CDS) readout architecture [10, 11, 12] and on-chip amplifier. Each column contains a CDS sensing scheme with two separate sample and hold branches for signal and reset levels. These signals are read out differentially, allowing CDS to suppress the fixed pattern noise (FPN) due to the threshold voltage non-uniformities of

the in-pixel amplifier transistors, and to reduce the low- frequency noise (1/f) generated by the source follower MOS transistors [10]. CDS also reduces the kTC noise of the floating diffusion node in the PG pixels since the signal sense node is different from the signal integration area. A crowbar switch (CB) when pulsed shorts the sampled signals during the readout cycle to reduce column FPN. The major source of noise in this circuit is thus the kTC noise introduced by the sample and hold capacitors, since the kTC noise from the PG pixels is suppressed by the differential output technique. Fixed pattern noise can be further suppressed by subtracting a full dark image from an illuminated one. Testing of this device will include wafer-level screening to identify candidate imagers for preliminary characterization and packaging. Pixels will be evaluated for dark signal, conversion gain, and quantum efficiency at specific wavelengths.

X-ray testing on screened parts will be performed at MIT CSR. We also propose to irradiate several examples of this APS device with protons characteristic of the trapped radiation belts and solar flares.

6.1.2 High responsivity output amplifier evaluation

One of the intriguing features of the I/SOI-CMOS process is that the minimum gate length, 0.35 μm, is much smaller than that of the standard CCD process. Moreover, the lithographic capabilities in the Lincoln Microelectronics Laboratory include advanced steppers which can resolve features down to 0.15 μm. An APS charge sensing circuit scaled down to these feature sizes would have substantially lower capacitance, and potentially even better noise performance than could be achieved with CCDs. To explore the properties of circuits made with such fine geometries we have included on the mask set a small imager with the output circuits scaled to the minimum feature sizes allowed by the process. Figure 10 illustrates the relative sizes of the standard CCD output circuit and the scaled version on I/SOI Development Lot.

As is discussed in detail below, we expect the smaller size of the transistor, and the resulting lower capacitance, to lead to a much higher responsivity, and, possibly, much lower noise than the conventional CCD amplifier. In this layout the CCD channel and reset FET are located in the bulk handle wafer, while the sense FET is made in the SOI layer. We propose to take advantage of the flexibility in CCD clocking to characterize the noise of this output stage as a function of sampling rate. Versions of this device using n-channel and p-channel SOI-MOSFETs have been designed and both will be characterized.

The noise of discrete SOI CMOS transistors from the Developoment lot will also be evaluated as a part of this task. In particular, the Development mask contains a number of alternative approaches for controlling floating body effects in SOI transistors. As we discuss below in Section 6.2.1, these alternatives will be compared to determine which provides the best noise performance.

6.2 Task 2: Design Studies for an Active Pixel X-ray Imager

The data obtained from the Development Lot test structures will be used to address a number of questions which must be answered before the detailed layout of a next-generation imager can begin. These questions can be organized into two categories: noise reduction and charge collection efficiency. We note that these are precisely the two areas where our proposed device differs most significantly from current CMOS APS design practice. We summarize these proposed design studies in the remainder of this section.

6.2.1 Noise considerations

Low-noise Transistor Design

The design of low-noise charge-detection circuits for CCDs has been treated in several publications, and the same considerations carry over to APS devices. A fundamental relation governing the noise performance of floating diffusion (as well as floating gate) output circuits using a

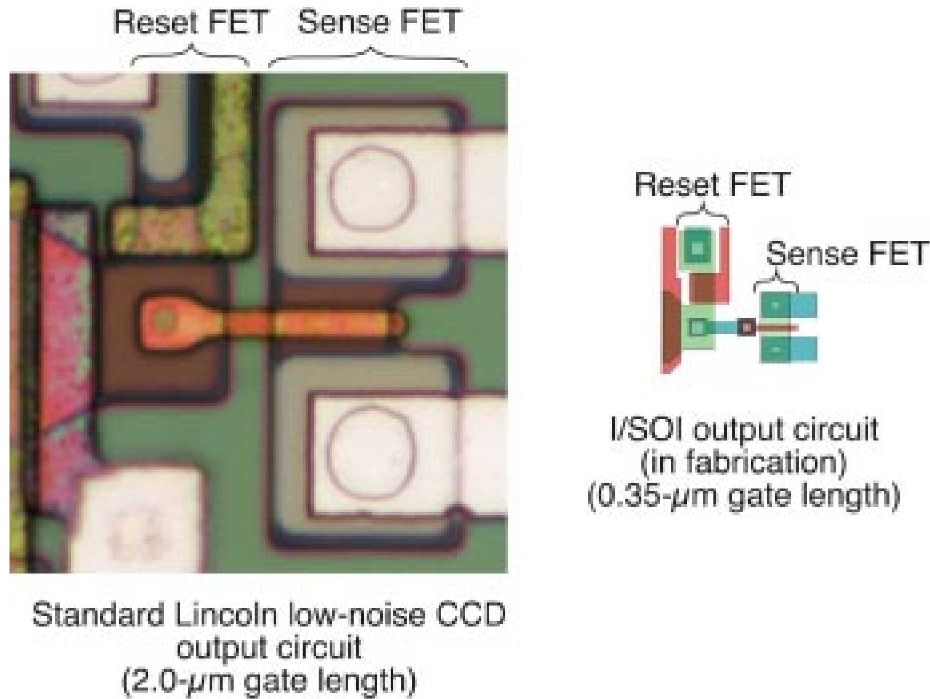

Figure 10: **Photo of the standard CCD output circuit made with 2-μm design rules (left) and computer drawing of the scaled output circuit using 0.35-μm design rules and currently in fabrication as part of the "Development" lot (right), shown at the same scale.**

source follower was given by [13]:

$$N_e = \frac{e_n(f)C_t}{q}\Delta f \qquad (1)$$

where N_e is the rms noise electron count, $e_n(f)$ is the noise voltage of the sense transistor at a frequency f (usually the serial clock frequency), C_t is the total capacitance at the sense or charge-collection node, Δf is an effective system bandwidth dictated by the downstream video processing including correlated double sampling (CDS), and q is the electron charge. Another measure of circuit performance is the responsivity R, or the conversion gain from electrons to volts, which is given by:

$$R = \frac{qA}{C_0} \qquad (2)$$

where A is the source-follower gain and C_0 is an effective sense-node capacitance (C_t but with the FET gate-source capacitance reduced by the source-follower feedback). One obvious message from Equation 1 is that for best noise performance the total sense-node capacitance must be minimized, and this drives the CCD designer to use the smallest possible geometries consistent with the process design rules as well as various tricks to minimize parasitic capacitances [14]. A small capacitance also yields a high responsivity R, which means that a small charge packet is converted to a high sensor output voltage, well above the noise floor of the external analog sources. For the standard Lincoln CCD process, as used for the Chandra/ACIS sensors, the minimum geometries were 2.0 μm, and this resulted in $C_t \approx 5$ fF and $R \approx 15 - 20$ μV/e$^-$. The techniques described in [14] have been employed in a variety of other Lincoln imagers, some employing two-stage source- follower amplifiers for operation at higher data rates. A summary of the best noise performance of these devices as a function of readout frequency is shown in Figure 11. Note that at our target of data rate of 10^6 pixel s^{-1}, these existing amplifiers are already capable of the noise performance we require. When coupled with the highly parallel APS readout archi-

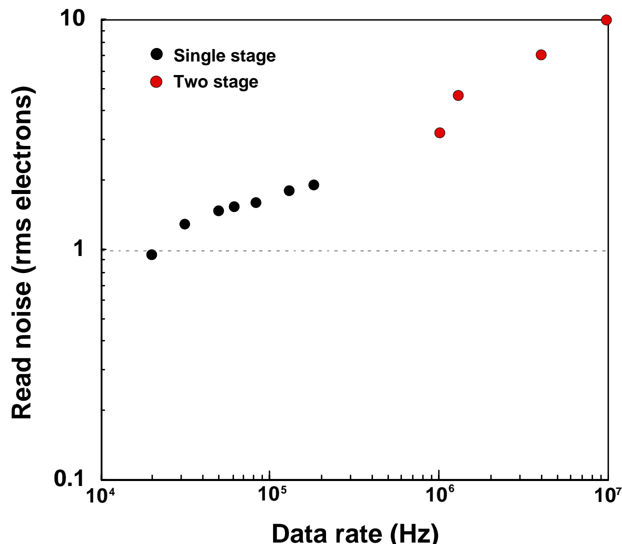

Figure 11: **Measured noise vs. output data rate from a variety of CCDs made using the standard Lincoln Laboratory CCD process.**

tecture, we conclude it should be quite feasible to obtain low noise at high frame rates.

Note from Figure 10 that the I/SOI process allows a dramatic reduction in the size of the sense transistor. It can be immediately appreciated that the reduced size of the I/SOI version should have a much lower C_t and higher responsivity R, and, potentially, even lower noise than the larger CCD amplifiers.

The major unknown in estimating improvements in noise performance with sub-μm circuits is the noise term e_n in Equation 1. In conventional CCD processes the thermal and 1/f noise components in e_n are fairly well characterized, but in SOI-CMOS transistors there are new issues to deal with. Whereas in bulk CMOS devices unwanted charge in the body can escape to the substrate or to a well contact, in SOI technology there is no conducting substrate. If contacts to the body are omitted, unwanted carriers in the body (such as holes in an NMOS device) can charge the body and change the effective threshold voltage of the transistor through the backgate effect. This process is known as the floating body effect. In addition, a CMOS active pixel sensor must contend with additional circuit noise sources such as the access transistor and column amplifier noise.

The particular detector isolation advantages of this unique SOI architecture, however, are well-suited to suppression of these additional noise sources. The compact design enabled by mesa-isolated FDSOI transistors and the 0.25 μm lithographic patterning in fabrication vastly decreases parasitic contributions to the sense node capacitance. Since the peak drain electric field is lower in FDSOI transistors than in bulk devices, there is less hot carrier generation. For similar reasons, the floating body effect is reduced in FDSOI relative to PDSOI, and can be reduced further with body contacted devices. Body contacted layouts also provide the advantage of suppressing the parasitic edge leakage with minor layout area penalty. Transistor biasing at the edge of the subthreshold region of operation will reduce contributions from impact ionization and techniques such as forward body biasing have been seen to improve the low-frequency noise performance of PMOS transistors [15]. As noted above, the Development Lot mask set has a variety of n- and p-channel FETs, both with and without body-contacted layouts. Our Task 1 characterization of the noise properties of these devices will guide our design choices in Task 2.

Low-noise pixel design and CDS

To obtain the optimum noise performance from an APS we must use correlated double sampling (CDS) to remove kTC noise and suppress low-frequency 1/f noise. In an APS this can done either in the pixel itself or in each column readout circuit. This section discusses the tradeoffs of the two approaches. In correlated double sampling the output signal is constructed from the difference of two measured voltages. The first is the voltage of the readout circuit after a reset operation but before a charge packet is delivered to the sensing node. This voltage contains the kTC noise resulting from the reset operation and must be subtracted from the voltage obtained after the charge is transferred to the sense node. In Figure 9 the section labelled column readout illustrates the circuitry needed to perform CDS on a per-column basis. This column-readout-based CDS can only be used by the photogate-type

pixel. This circuit cannot be used by the photodiode pixel illustrated at the top of this figure because there is no practical way to store the pixel reset level. For the photodiode pixel, then, the CDS must be performed inside each pixel, which means additional FETs and storage capacitors. We conclude that the photogate pixel, though slightly more complicated than the photodiode pixel, is likely to be the preferred path to a high-performance APS.

Several other design issues need to be resolved in order to come to a complete understanding of sensor noise. These include not only the noise of the pixel-level circuits but also the noise of the column amplifiers and CDS circuits. These will be studied by suitable test circuits that enable separate evaluation of each noise contribution.

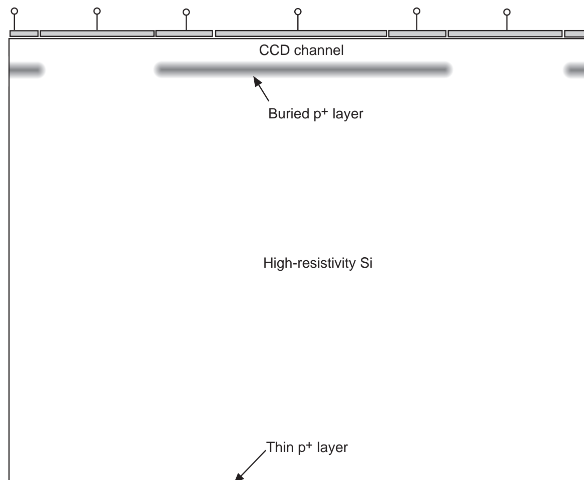

Figure 12: **Cross section of a CCD with a buried p+ layer for directing photoelectrons to selected regions of a CCD.**

6.2.2 Charge collection efficiency

The I/SOI-CMOS process is, as mentioned previously, unique among CMOS processes in allowing the use of a thick, high-resistivity substrate as the photon detection medium. However, in order to fully collect photoelectrons from an x-ray event we need to tailor the substrate E-fields to direct the carriers to the photogate and not be lost to recombination at, for example, the buried oxide/substrate interface. A closely related problem has been studied at Lincoln, and the solution has direct applicability to this device. Figure 12 illustrates a cross section of a back-illuminated CCD on high-resistivity material, and Figure 13 shows the results of a simulation of this device under bias. This device required a scheme by which all the photocharge could be funneled to a particular pixel. The solution consists of implanting a buried p+ layer everywhere except beneath the gate that is to collect the charge. Such a layer forms the basis of an electronic shutter that was invented at Lincoln and has been used on several devices([16]. The p+ layer deflects photoelectrons, while the field from the collecting gate is able to draw carriers through the opening in the layer. Figure 13 shows the potential distribution in this device with 12 V between the collecting gate and the back p+ layer. The bulk is fully depleted, so there is no neutral region where carrier diffusion or recombination loss can occur, and the potential profile shows that all photoelectrons, regardless of where they are generated, are drawn through the opening the p-barrier layer. We propose to adapt this approach for used in our demonstration APS.

6.2.3 Integration of signal processing functions.

CMOS technology offers a rich variety of functions that can be integrated on the detector and thereby reduce the processing or computational load on off-chip circuitry. One of the obvious major components we will examine is the A/D converter. As mentioned previously, a commercial APS with over 2000 columns and a 10-bit converter on each column is currently in production [2]. We propose to include prototype A/D designs on the photomask for evaluation purposes.

Although an A/D on each column offers a very high degree of parallelism and processing throughput, it may make more sense in this application to take a different approach. X-ray photon counting data are extremely sparse; in raw Chandra/ACIS CCD frames, for example, fewer than 5% of the pixels contain detectable

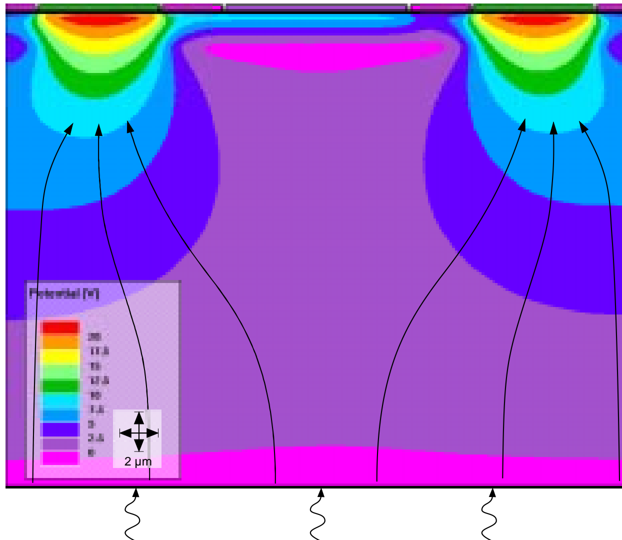

Figure 13: **Simulated potential profile of the structure of Figure 12 with 12 V across the device.** The bulk is fully depleted, and the field profile ensures that all carriers will be directed through the openings in the p+ layer.

signal, and of those only about 10% (i.e., < 0.5% of all pixels) contain signal from interesting X-ray events. These characteristics suggest that digitizing every pixel is a waste of power and die area, and that identifying and digitizing only those pixels with measurable charge would make more sense. We will examine pixel and readout circuitry designs in which pixels containing significant charge are identified before fine digitization, so that the peripheral circuitry can then address, read and digitize only the pixels of interest. The data rates for this process may be so low that a small number of A/Ds will suffice for an entire chip while still offering a short effective frame time.

6.3 Task 3: Demonstration Device Fabrication and Test

The final task in our program is to apply the results of our device testing and of our architecture studies to the design and fabrication of a demonstration APS. The details of the design will depend on what is learned in in Tasks 1 and 2, but we anticipate that we may wish to fabricate more than one candidate pixel design.

Data and analysis from the Development Lot APS will be used to evaluate and modify I/SOI design rules and implantation steps. A new mask layer and process module will be created for the deep implant. This process module creation may require a short loop fabrication experiment to verify the simulations.

Candidate pixel designs will be laid out with the updated design rules using the three-level metal routing available in the I/SOI process. These pixel designs will be incorporated into active pixel imagers with necessary decoder and pad buffering circuitry. Test circuits to aid in characterization of APS array (e.g. discrete photodiodes and floating gate structures) will also be laid out. Additional structures on the mask set will be the necessary photolithography resolution and alignment measurement features and a test strip with a standard array of transistor sizes, contact chains, and other process monitoring devices.

The X-ray imaging APS will be fabricated on custom high resistivity (> 3000 Ω-cm) bonded silicon-on-insulator wafers using 28 lithography steps. These steps include a new buried p+ implant for the sense node, two polysilicon layers, all plasma etched features for precise critical dimension control, and a fully planarized three-layer metal back end with stacked vias.

The resulting APS sensors will be tested at MIT Lincoln Laboratory and at MIT CSR. We will evaluate noise for each pixel design as a function of sampling rate, for rates in excess of 10^6 pixel s^{-1}. We will characterize X-ray detection efficiency of these front-illuminated devices at energies from 0.5 to 10 keV as a function of photogate bias to determine effective depletion depth. We will also determine dark current as a function of device operating temperature. Finally, we will characterize the effects of both non-ionizing and ionizing radiation on sensor performance.

Our demonstration lot will produce eight 150-mm-diameter wafers. Our die size is 22 mm and we expect the yield to be sufficient that we can reserve a number of wafers for use in follow-on programs. As noted above, these devices could be converted, with additional processing, into

back-illuminated sensors. Thus one especially interesting follow-on from this program would be to complete back-surface treatment of selected wafers and test them in a back-illuminated mode.

7 Management Plan

This project will be executed by a small, experienced team at the MIT Center for Space Research and MIT's Lincoln Laboratory. The investigators have worked closely with one another for at least ten years, and no special management problems are expected.

The Principal Investigator, Dr. Marshall Bautz, will be responsible for the successful completion of the project, and for the allocation of project funds. His progress will be monitored by Dr. Jacqueline Hewitt, the Director of the MIT Center for Space Research.

Lincoln Laboratory is an FFRDC operated by MIT for the U.S. Air Force. CSR, on the main campus of MIT, and Group 87 of the Lincoln Laboratory have been involved in the joint development of detectors for use in NASA-sponsored X-ray Astronomy missions for the past 15 years, beginning with ASCA in 1988, and extending through Chandra/ACIS, HETE, ASTRO-E, and ASTRO-E2.

Although all personnel at Lincoln are MIT employees, the facilities were provided by, and are owned by, the Air Force. Formal approval of the Air Force for the use of these facilities will be requested after selection. The contract between MIT and the Air Force allows the use of these facilities to assist main campus activities provided, in the case of an open, Government-sponsored competition such as the ROSS, that the sponsoring agency certifies that no US company proposed the same effort. If our proposal is accepted, we will request such a letter from the discipline scientist at NASA (Dr. Lou Kaluzienski). Funding for the Lincoln effort would be provided via an Inter-Agency Transfer of funds between NASA and the DoD. To date, no request for the use of the Lincoln facilities for NASA contracts or grants has ever been denied.

We expect to complete Task 1 (see Section 6 for task definitions) by the end of month 6. Task 2 will begin about month 6 and will be completed by month 18. Design work for Task 3 will begin in month 18, wafer fabrication for this task will span months 24-30, and months 30-36 will be devoted to characterization of next-generation APS devices.

8 Investigator Roles

The Principal Investigator is supported by four Co-investigators at MIT CSR and two Co-Investigators at MIT Lincoln Laboratory. The roles of each investigator are described here:

Dr. Marshall Bautz, the Principal Investigator, is responsible for the technical direction and completion of the investigation. He will coordinate the work of the co-investigators, and assume final responsibility for technical decisions.

Dr. Barry Burke, Co-investigator, (MIT Lincoln Laboratory) will be repsonsible for design of low-noise sense and readout circuitry. He will consult on process development and device physics and operations issues.

Dr. John Doty, Co-investigator, will consult on interpretation of test results, and assist in optimizing both test system and device operating characteristics for minimum electronic noise.

Dr. Steve Kissel, Co-investigator, will take resonsibility for laboratory testing of the devices of APS devices at CSR. He will also conduct radiation tests.

Dr. Gregory Prigozhin, Co-investigator, will consult on issues relating to APS sensor design and fabrication. He will help design the X-ray performance tests, interpret the test results and recommend fabrication process modifications.

Dr. George Ricker, Co-investigator, will advise on the interpretation of X-ray test results.

Dr. Vyshnavi Suntharalingam, Co-investigator, (MIT Lincoln Laboratory) will be responsible for overall APS design and fabrication, and will supervise testing at Lincoln Laboratory.

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1 Appendix: Detector Fabrication and Characterization Facilities